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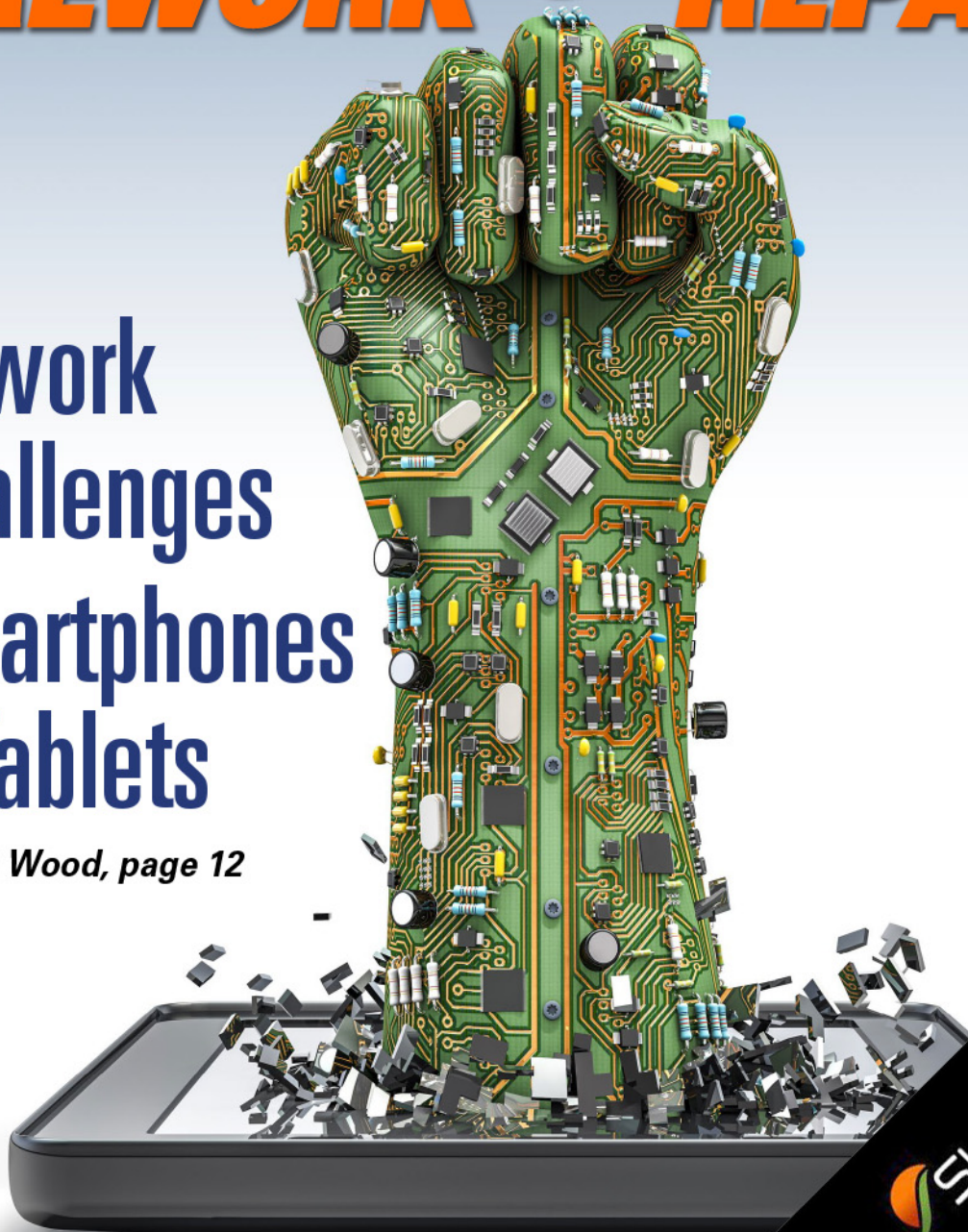
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## REWORK & REPAIR

### Rework Challenges Smartphones & Tablets

by Paul Wood, page 12



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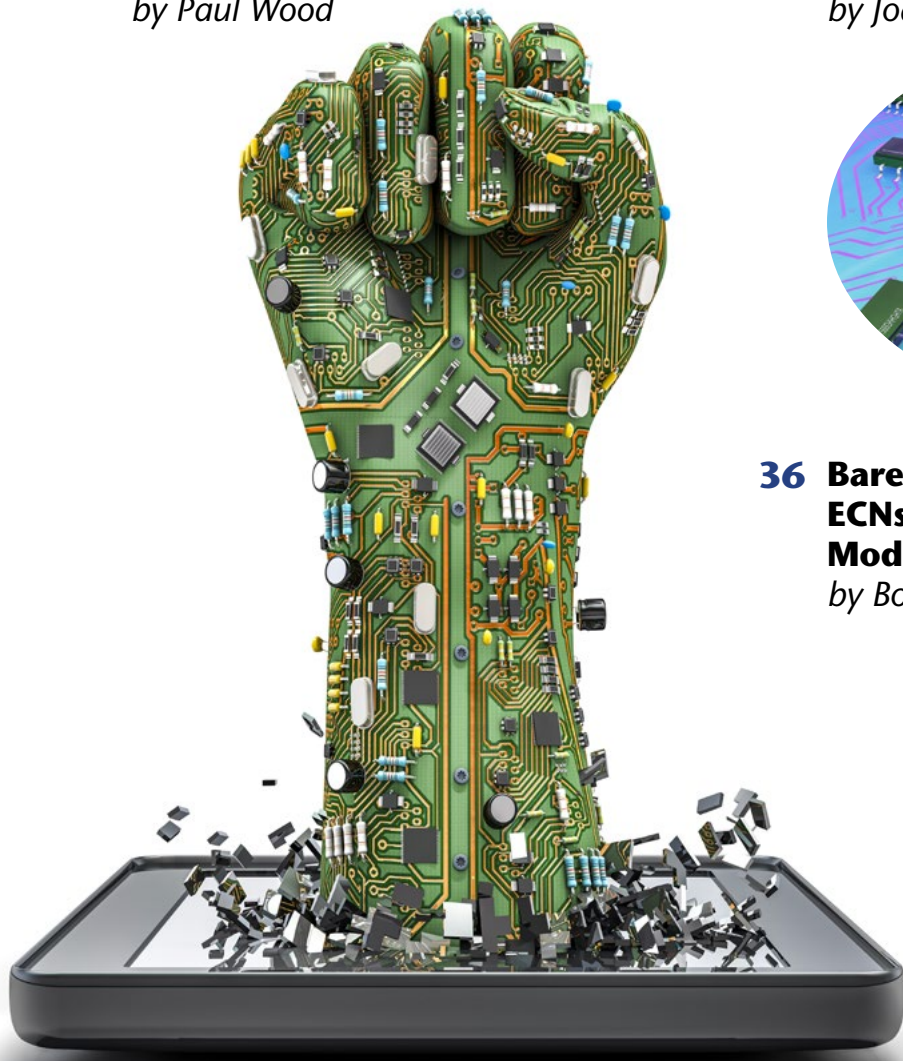
## November 2014 Featured Content

### REWORK & REPAIR

PCB assembly rework and repair are often seen as afterthoughts, and they're not particularly sexy or exciting topics, either. But when your parts are too pricey to be scrapped, rework and repair can be lifesavers. This month, expert contributors Paul Wood, Bob Wettermann, and Joerg Nolte offer updates on the latest rework and repair processes and equipment.

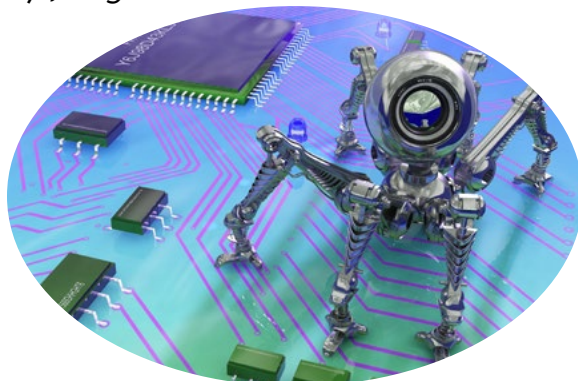
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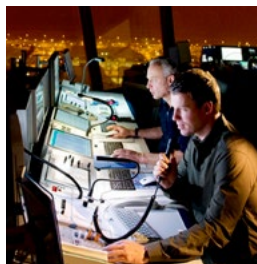
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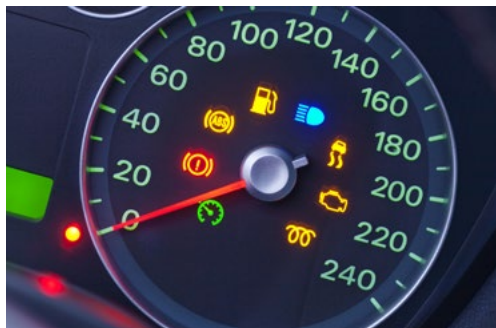
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## THE WAY I SEE IT

# IPC Seal of Approval

by Ray Rasmussen

PUBLISHER, I-CONNECT007

What if we could get the military, aerospace, medical, automotive, and a few other industry groups to agree to accept one site audit and one certification? In other words, one audit, once a year, which covers everything.

Already underway, IPC has ventured into the area of PCB fabricator and EMS provider audits based on IPC-1071 for fabricators and IPC J-STD-001 and IPC-A-610 for PCBA. Called [IPC Validation Services](#), this effort is being driven by IPC's OEM members who want to replace for individual site audits with a single IPC audit as the standard for vendor acceptance.

## What Does Compliance Cost?

Randy Cherry is leading this effort at IPC. It's a good first step but it doesn't go far enough IMHO (my kids taught me that). We have an opportunity to remove a huge source of pain

and suffering for many companies on both sides of the transaction. These site audits are time-consuming and expensive. After querying, I found one medium-sized EMS company's costs of compliance, including audits, translated to about 0.5% of sales. I'm sure that with some economies of scale, that number would decrease, but it's still a significant number for most companies and another non-value-added expense to doing business. EMS industry wide, that starts to add up. At about \$500 billion in sales, the EMS industry's cost of compliance is approximately \$1–3 billion annually. If the same number holds for PCB fabs, then we're looking at another \$100–300 million. The industry spends a ton of money on this! Get this down to a single audit and the OEM wins, EMS/PCB fabs win, and if IPC does the job, they win as well. Seems like a no-brainer. Here's a list of





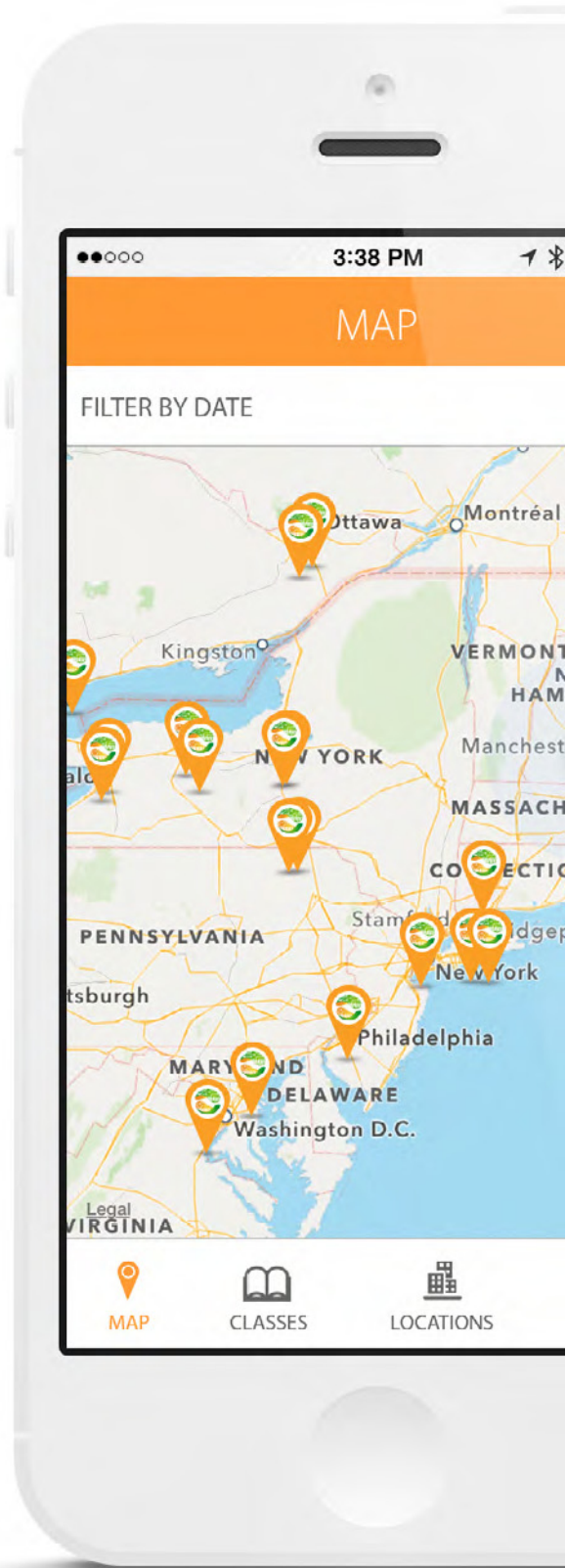
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**IPC SEAL OF APPROVAL** *continues*

likely target certifications which could be addressed with this effort:

- ISO 9001 (Quality)
- ISO 14001 (Environmental)
- ISO/TS 16949 (Automotive)
- ISO 13485 (Medical)
- AS 9100 (Aerospace)
- ANSI/ASQ Q9001
- ANSI/ASQ Q9003
- DSCC (Defense Supply Center Columbus)/DLA (Defense Logistics Agency)
- NADCAP (list specifications and/or audit type)
- UL
- ITAR (Registered #)
- OHS18001 (Occupational Health & Safety)
- IRIS (International Railway Industry System)
- MIL PRF 55110

I'm sure there are more we could add to this list and some that shouldn't be on it. In any case, you get where I'm going with this.

**It Will Take a While**

I figure we can make a 10-year plan to address the consolidation of all these different efforts. If we start off with a more comprehensive and complete audit with ongoing product and site reviews than what the current agencies do themselves, it might be an easy call for them to sign on. We should be so much better (and cheaper, for them), which will "pressurize" them (I love that word) to join up.

We just need to go slow at first, proving IPC's capabilities to do this properly, one step at a time. The IPC board would have to commit serious resources to this effort and think long-term. There will be a payback for the IPC, but it may take a couple years of investment to ensure this is done properly. A half-assed effort will just add another layer of audits to the industry, which won't do anyone any

good. Theoretically and technically, it doesn't seem to be something outside the capability of IPC. They know the industry inside and out. Politically, we may find some roadblocks, as all these certification groups fight to protect their turf. That's why we need to go slow and methodically, based on a long-term plan designed by the stakeholders.

**Making this Painless**

In thinking this through a bit, I believe one of the best ideas is to make this IPC audit and *seal of approval* a no-brainer for companies, sort of like the Malcolm Baldrige National Quality Award. Most companies that go down this path get more out than they put in, meaning this: The improvements they make as a result far outweigh the cost. That's the way this should be. The assessment should provide objective feedback, at some level, to those being audited. A CEO should welcome the audits each year, which should point out problems and possible solutions, provide benchmarking data and a corrective action schedule. It shouldn't be punitive, but rather, constructive.

They should know that if they stumble, IPC will work to help them come into compliance. It certainly has to be IPC's goal to get as many members into compliance as possible. And since companies have to be members to be audited and OEMs have to be members to get access to the audit company's information, IPC membership grows as well.

**Different Levels**

At first, I thought that it might be nice to have two or three different levels: bronze, silver and gold. Then, I reconsidered. What is needed is one comprehensive audit allowing all companies who pass to build any type of product. It should be so good that in order to sell PCBs to any serious OEM, you need IPC's seal of approval. This does a couple things. It ensures that IPC-certified member companies are recognized worldwide

“  
***The IPC board would have to commit serious resources to this effort and think long-term. There will be a payback for the IPC, but it may take a couple years of investment to ensure this is done properly.***  
”



IPC SEAL OF APPROVAL *continues*

as the best of the best. And, it enhances IPC's importance in the eyes of the OEM community, including the military and governments around the world. It sets the standard.

### Some Precedence

In 1999, PCB007 was a business built around transaction management for the PCB industry, which I was part of. PCB007 had a similar business model: to audit fabricators worldwide to a standard that would eliminate the need of OEM audits. Both the OEMs and the fabricators loved the idea of single audits to replace the expense of continually auditing or being audited. In fact, many of the very large OEMs we visited hadn't audited their PCB supplier in years. The idea of an annual audit at no cost to them was intriguing as long as we were looking at the right stuff—and we were. At the time, we had Rob Scott, a longtime PCB fabricator, conducting the audits. He knew much more about PCBs than the OEM auditors did. He would see “behind the veil.” They liked that.

The transaction side of that business became a casualty of the dotcom bust, but the news site continued on, when my partner and I purchased the assets of the business in 2004.

### Conclusion

At this point, I don't see a downside. Sure, there are quite a few potential roadblocks, but IPC has the clout to pull this off. If the IPC board can see the bigger picture and make a long-term investment in this effort, the industry wins. **SMT**



Ray Rasmussen is the publisher and chief editor for I-Connect007 publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine*. To read past columns, or to contact

Rasmussen, [click here](#).

## Video Interview

# Mentor Fine-Tunes its Consulting Operations

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Jay Gorajia, director of consulting at Mentor Graphics, joins Editor Ray Rasmussen to discuss the creation of a consulting organization to help customers extract value from their existing assets. The organization's main goal is to help small- to medium sized companies—those who don't continually buy or expand capacity—make the best of what they already have.



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# Rework Challenges FOR Smartphones & Tablets



**by Paul Wood**  
OK INTERNATIONAL/METCAL

Smartphones are complex, costly devices and therefore need to be reworked correctly the first time.

In order to meet the ever-growing demand for performance, the complexity of mobile devices has increased immensely, with 70% more packages now found inside a mobile device than just a few years ago. For instance, a 1080P HD camera with video capabilities is now available on most high-end smartphones or tablet computers, making their production more elaborate and expensive.

The printed circuit boards for these devices are no longer considered disposable goods, and their bill of materials start from \$150, with

higher-end smartphones going up to \$238, and tablets well over \$300.

The implementation of the surface mount devices is crucial for smartphone manufacturers, offering increased component density and improved performance. For example, the newer style DDR memory integrated components use less power and work at twice the speed of former versions. It is not surprising that most component manufacturers now produce these surface mount devices as small as 1 mm square.

Mobile products generally use an epoxy underfill to adhere components to the printed circuit board in order to meet the mechanical strength requirements of a drop test. Reworking glued components is the most difficult application in the electronics industry, and must be addressed as a process.





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**REWORK CHALLENGES FOR SMARTPHONES AND TABLETS** *continues***Rework Challenges**

The removal of a glued component from a PCB assembly requires a specific order of operations. The first step is to remove the glue fillet (Figure 1) located between the component and the circuit board. Mobile products generally have many types of components glued to the PCB in order to meet the industry standards outlined in JESD22-B111 Board Level Drop Test Method of Components for Handheld Electronic Devices and JESD22-B110 Subassembly Mechanical Shock. The epoxy is applied to the components to prevent the common failure modes of cracks in the laminate, cracks near the intermetallic, and cracks in the bulk solder. The addition of the epoxy increases the robustness of the design and enhances reliability for the user.

One of the issues associated with underfill epoxy is the glass transition temperature of the material. The glass transition temperature is the temperature at which a sudden change of physical properties occurs. In the case of underfill epoxies, they generally soften at approximately 208°C (exact temperatures dependent on manufacturer's specifications). Lead-free solder, used to form an intermetallic bond between the component and the pads attached to the circuit melts at 217°C with peak temperatures of 235°–245°C common. The closeness of the epoxy and solder temperatures creates a narrow window of opportunity for removal of the ep-

oxy and removal of the component. Removal of the surface mount device requires the removal of the epoxy fillet from around the sides of the device without damaging or disturbing the adjacent discrete components. Failure to remove the fillet increases the chances of damaging or removing the adjacent components (Figure 2) adding time and cost to the rework process.



Figure 2: Adjacent components within 10 mils of SMD.

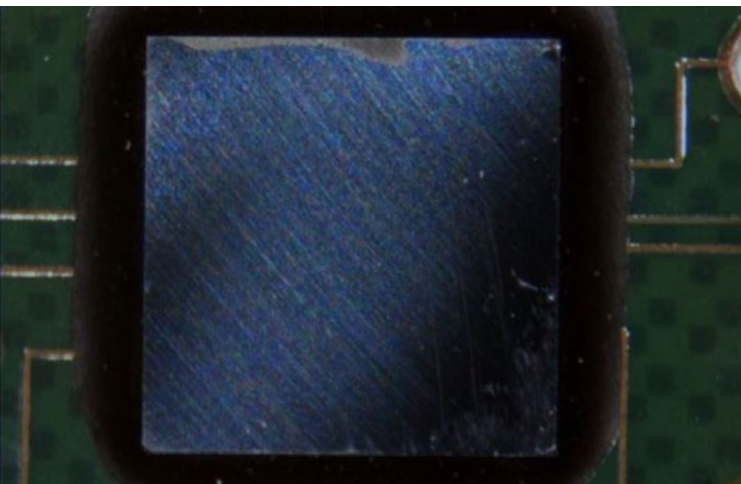


Figure 1: SMD with epoxy fillet.

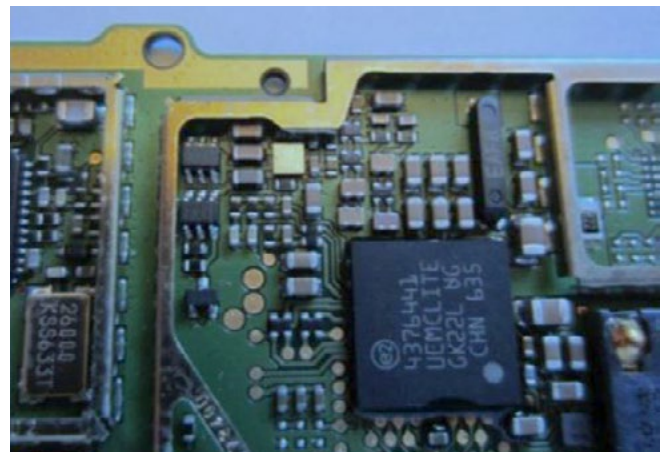


Figure 3: Densely packed components commonly in use for mobile devices.

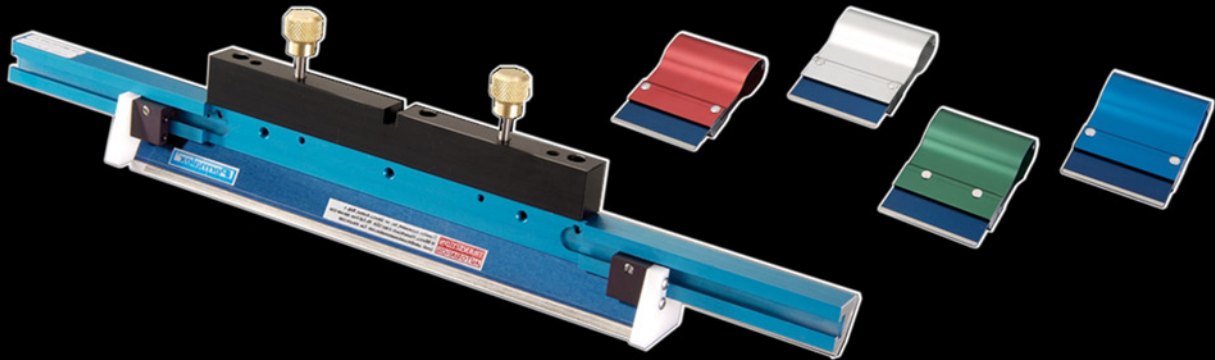


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An example of an epoxy fillet removal technique for package-on-package (PoP) or ball grid arrays (BGA) is the use of a handheld convection tool and dental picks, or the use of a soldering iron with very small solder tips. The dental pick or solder tip is heated and then used to carve the epoxy away from the component. This process requires a skilled operator as no automation process exists. To facilitate the ease of carving the epoxy, the dental pick tip must be polished to a mirror finish using extremely fine grit sandpaper. The polished tip, when heated, will achieve the temperature needed to change the physical properties of the epoxy. Even a skilled operator cannot guarantee success in removing the epoxy fillet. Care must be taken to ensure that the tool does not damage the surface of the PCB, component to be removed, or adjacent components.

The next step is to remove the component from the PCB by using infrared or convection to heat the board and a retractable vacuum nozzle or other mechanical means, like a tweezers nozzle, to physically remove the component. In densely packed mobile devices, BGAs are often mirrored on the PCB. Removal of the top BGA requires precision control of the temperatures. If the solder on the bottom BGA becomes liquidous at 217°C during the top BGA's removal profile, the solder underneath the bottom BGA expands in volume, forcing the solder to ooze at high pressure through the softened epoxy which has exceeded its glass transition temperature. This can be seen as small solder balls that have appeared out of the BGA (Figure 4).

The result of this phenomenon is the appearance of a poorly executed surface mount reflow process, and the possibility of functional failures as shorts. When an X-ray inspection is conducted and compared to original solder joints, a difference in size can be seen between the original printed circuit board and the circuit board after rework. The bottom BGA now has opens as solder has been lost. The solution is to keep the bottom chip below 217°C. 208°C, in general, is the ideal rework temperature for most parts. This often requires the use of a spot heater in the preheater to locally heat and cool components in a vertical position during rework. With the correct temperature applied to

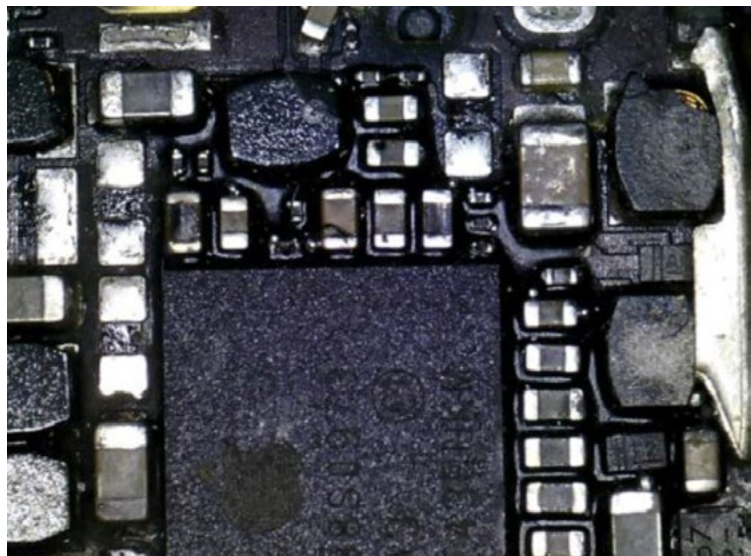


Figure 4: Solder expelled through epoxy during removal.

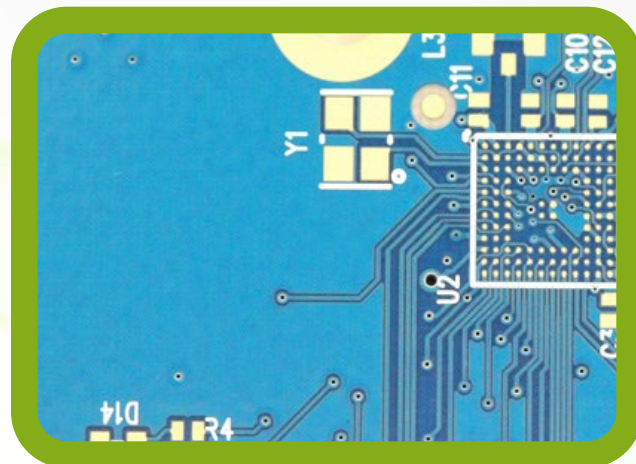
the bottom BGA, the top part can be reworked at lead free temperatures. At this point, the choice must be made to scrap the part or recover the component for later reuse.

Some production-level manufacturers reclaim components, or reball and reuse some parts because of cost (e.g., memory, processors, and Wi-Fi chips). Energy-efficient and faster DDR memory costs up to \$35 each, while processors can also cost up to \$35 apiece and NAND flash memory and Wi-Fi chips often costing as much as \$41 each. PoPs with both processor and memory are up to \$50 combined. The cost of these components can represent a significant portion of the cost of the PCB. If a PCB is damaged due to poor rework operations, some money can be reclaimed from refurbishments of the high cost components. Reusing components after removal is a hidden operation, often kept from most OEM manufacturers.

However, contract manufacturers recycle parts as a cost-savings measure. Removal and reuse of components is common in the development lab environment. Component cost for a prototype may be high and the time needed to acquire a new part may exceed the time available which increases development time and costs. This is true in and out of warranty rework markets. If they are to be reused, the compo-



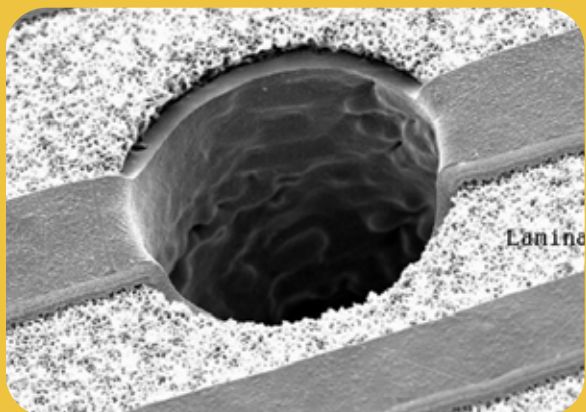
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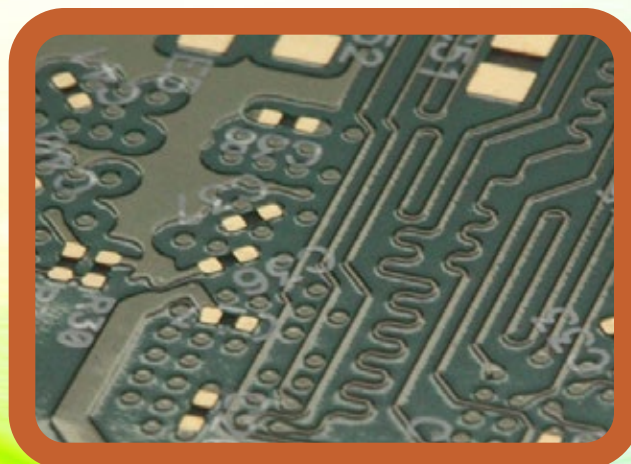


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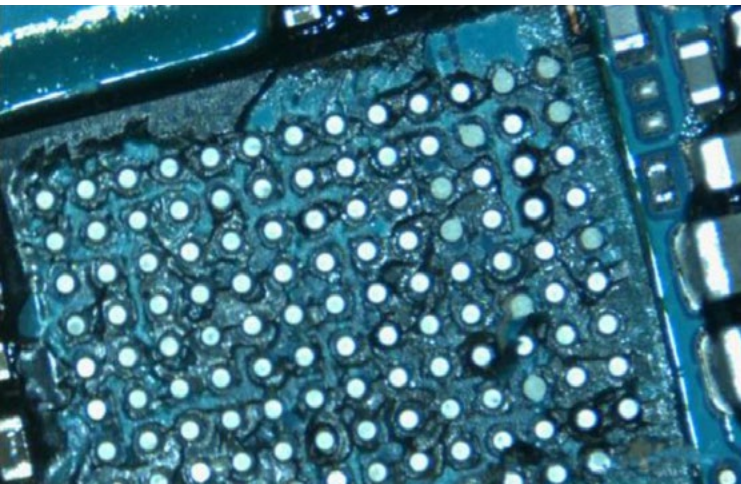
**REWORK CHALLENGES FOR SMARTPHONES AND TABLETS** *continues*

Figure 5: Residual solder and epoxy.

nents must be removed safely at correct component temperatures. The pad area must now be prepared for a replacement component.

When a faulty component is removed from a PCB, solder and epoxy are left as a byproduct (Figure 5).

Residual solder and epoxy must be removed prior to component replacement. The most common way to remove residual glue is to scrape the epoxy using hand tools. Using this method greatly increases the risk of board damage. An alternative method is when the residual solder and epoxy removal operation can be done manually with a soldering iron, wicking braid, and flux (Figure 6).

Solder is cleaned with wick or retinned with soldering iron hoof style tips to level pads, in most cases, and in some cases increase solder heights on corners to stop bridges in the corners of a 0.4 mm PoP. This is because components are warped concavely in the middle as a new component, and might require this special technique to achieve success. The risks to the circuit board assembly are inconsistent solder removal resulting in poor adhesion, solder resist damage resulting in opens or shorts, and thermal damage to the PCBA. The alternative is less risk than the most common method. However, both manual processes add additional cost to the process due to the time and resources need to perform the pad cleaning operation and represent a risk to the manufacturing in terms of

scrap costs. Cleaning residual solder from ultra-fine pitch 0.35 mm and 0.4 mm pitch components now require a better solution known as contactless solder removal. Commonly referred to as scavenging, vacuum and hot air are used to melt solder and vacuum up solder without touching the PCB. The advantage of a scavenging site cleaning system is the equipment does not make contact with the circuit board reducing the risk of damaging the solder resist and pads. Scavenging systems require the same thermal profile controls as other rework equipment and benefit from automating the task of moving the vacuum collection nozzle over the site to provide consistent solder removal. With the solder pad cleaned, the operator is ready to replace the component.

Reattaching components to the PCB requires the use of either infrared or convection technologies to heat the board and a mechanical means of physically placing the component. The size of the components used in mobile devices provides a challenge to the operator. Processors have solder connections between 0.3 mm–0.5 mm (4–10 mils), micro-SMD component sizes range from 1 mm–6 mm square with 4 to 100 solder balls per package. Common solder ball sizes range from 0.1–0.2 mm (4–8 mils). Memory components are typically BGA

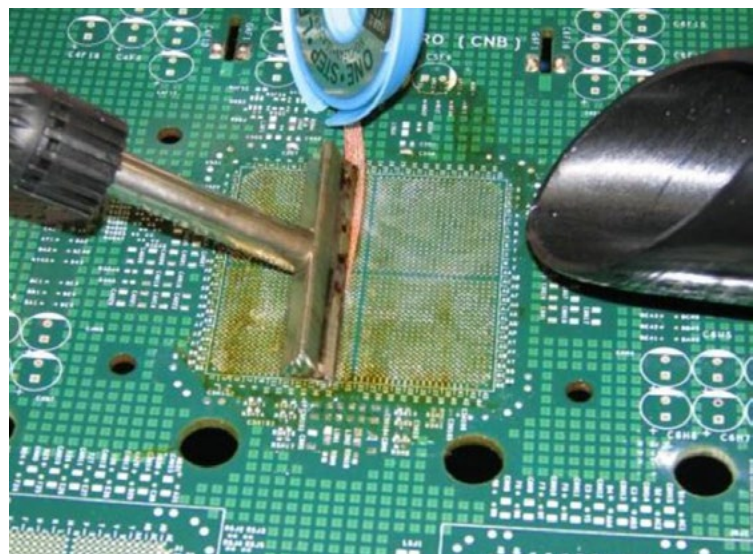


Figure 6: Pad cleaning using company soldering system and blade cartridge.



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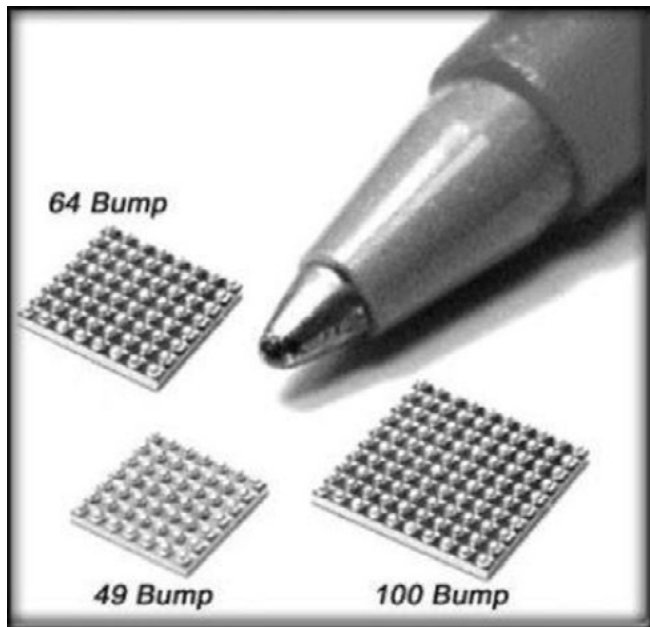
**REWORK CHALLENGES FOR SMARTPHONES AND TABLETS** *continues*

Figure 7: Micro-SMD examples.

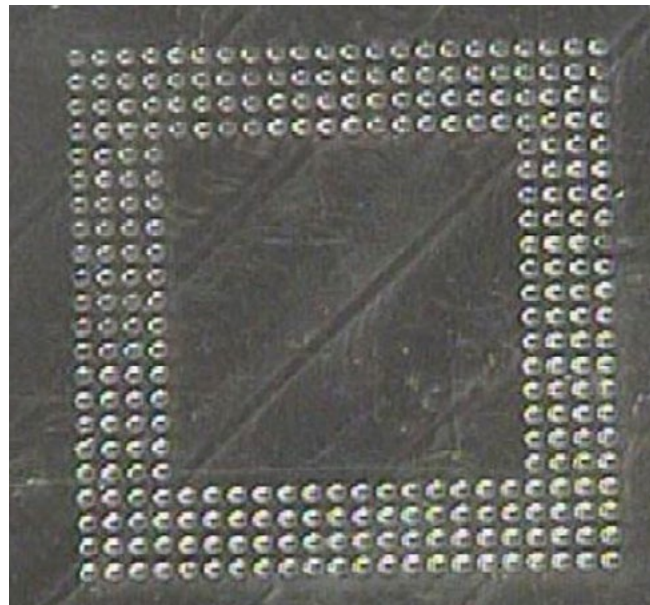


Figure 8: Repeatability of flux depositions on solder balls.

style and solder connections as low as 0.4 mm. Reattaching these components often requires the use of a camera to accurately align the part to the solder pad. There are a number of factors to consider when replacing components. The operator must consider whether to apply flux to the printed circuit board or to the component (Figure 8).

Liquid flux dries before the solder reflows. Gel flux, in paste form, is used during manufacturing and should be used during rework. Applying flux to the solder balls provides little coverage. Dipping the component into gel flux provides excellent coverage as well as solder ball cleaning. The ideal flux dip is half the height of the solder ball. This transfers the exact amount of flux onto the solder balls and not on to the PCB. After reflow, less contamination is present under the BGA. Also, flux does not drip through the via to the other side of the PCB. Other considerations include applying solder paste to the printed circuit board, usually not possible on mobile devices due to the densely packed components; screen printing the solder onto the components is possible on parts down to 0.4 mm pitch, or the easiest solution, dipping the components into solder paste. Each type of package presents its own challenge to the re-

work process. For example, component stencil printing is essential for successful rework of LGA, QFN, BTC, LLF, and PoP devices. Package on package requires the top and bottom components to be reworked simultaneously. These are processors and memory mounted on top of each other and are the most difficult to rework. Screen printing the solder paste onto the solder balls using a stencil is important to achieve the correct stand-off height. Flux dipping the balls of the top package is done to half the ball's height (Figure 9).

The PoP device is reflowed with a solder paste reflow profile. The placement of quad flat, no-lead (QFN/ BTC) components also require a repeatable process for rework. QFNs/BTCs, also known as leadless lead frame packages (LLF), have no solder on the package, but just a thin plated surface layer of tin, and the distance between the package and the circuit board is within 2 mils flat when soldered.

QFNs/BTCs require solder paste either on the PCB or on the part to be replaced. In mobile products printing the PCB is impossible because of high density to adjacent packages; the stencil would never fit to the PCB for printing. Stencils are made to print the package with 4 or 5 mils of solder paste. The center pad is a ground pad



**REWORK CHALLENGES FOR SMARTPHONES AND TABLETS** *continues*

and is usually split up into 4 or 8 quadrants; this helps stop the package swiveling during the reflow process and ensures solder coverage to be equal. Most manufacturers require 60–80% solder contact to the PCB ground pad in the center. This ground pad keeps the package cool and stops overheating, as heat is transferred to the PCB via the center ground pad. Special 0.4 mm pitch stencils have been developed to better align the package to stencil print locations. QFN/BTC with a pitch of 0.5 mm have been in mobile devices since 2005 and are much easier to rework. QFNs/BTCs with a 0.4 mm pitch are the most difficult and challenging. These components often have two rows of connections on the perimeter. Each type of component requires careful consideration in regards to the techniques needed to place the part on the circuit board.

Once the part is placed on the circuit board, the new components require the development of thermal profiles. Thermal profile repeatability is very important. The thermal profile should start with a linear ramp rate of 0.5°C–2.0°C/second which allows the gradual evaporation of volatile flux constituents and prevents defects such as solder balling/beading and bridging as a result of hot slump. It also prevents unnecessary depletion of fluxing capacity when using higher temperatures.

Next, an optional soak stage between 160°C and 180°C may be implemented for a few reasons. This includes minimizing the  $\Delta T$  across the board to <10°C and allows for full volati-

zation of the flux solvents to reduce flux induced voiding. Finally, the recommended peak temperature is 225°C–235°C and the total time above liquidous (TAL) should be less than 120 seconds above 217°C. A rapid cool down of 4°C/second is desired to form a fine grain structure. Slow cooling will form a large grain structure, which typically exhibits poor fatigue resistance. If excessive cooling 4°C is used, both the components and the solder joint can be stressed due to a high coefficient of thermal expansion (CTE) mismatch. Fixtures can be used to improve process yields. Fixtures are very important in mobile device rework due to the size and shape of many mobile device PCBs. A fixture will ensure consistency by locating the circuit board in relation to the heating source (Figure 11).

The fixture should be low mass and made of a material which does not act as a heat sink. A metal fixture will absorb thermal energy during use and will alter the profile. Proper circuit board profiling and the right fixture will ensure a repeatable process.

After the part has been reflowed, the circuit board is tested. Testing at this stage ensures the reworked component functions properly before applying the epoxy. Typically, the PCB will be subjected to detailed inspection and a

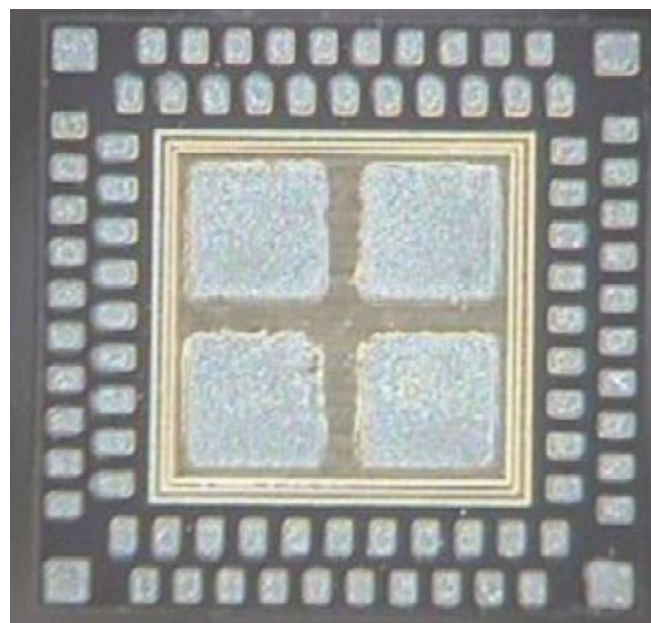


Figure 10: Multi-row QFN/BTC.



Figure 9: PoP/BGA paste dip.

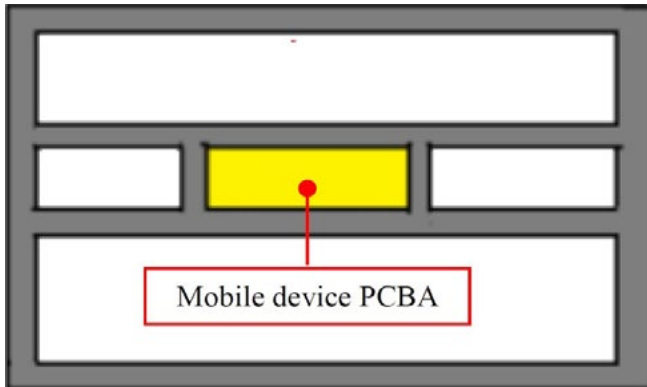
**REWORK CHALLENGES FOR SMARTPHONES AND TABLETS** *continues*

Figure 11: Mobile device fixture.

functional test. The detailed inspection insures that the component was placed and reflowed on the circuit board and that there is no observable physical damage to the board. Boards may be subjected to detailed visual inspection under magnification or subjected to X-ray analysis. The circuit board is functionally tested. This testing ensures the circuit board and the reworked part are functioning to specification and there are no opens or bridges as a result of the rework process. Once testing has been completed, the unit is ready for the final step in the rework process.

Finally, the last step in the process is to dispense epoxy underfill. Typically, the operator will use the epoxy defined in the manufacturing process. Generally, underfill is dispensed along a corner or in a line along the edge of the surface mount device (Figure 12). The device is heated to 125°C to 160°C in accordance with the manufacturer's recommendations and taking into account the circuit board properties. Capillary action will absorb the material and distribute it underneath the part filling the space between the component and the circuit board. The board is maintained at a constant temperature until the epoxy has cured. Typical cure time to achieve the optimal strength is approximately five minutes. However, the cure time can be longer depending on the epoxy properties.

### Considerations

After reviewing this article, readers will understand the challenges and processes needed for successful repair of surface mount devices

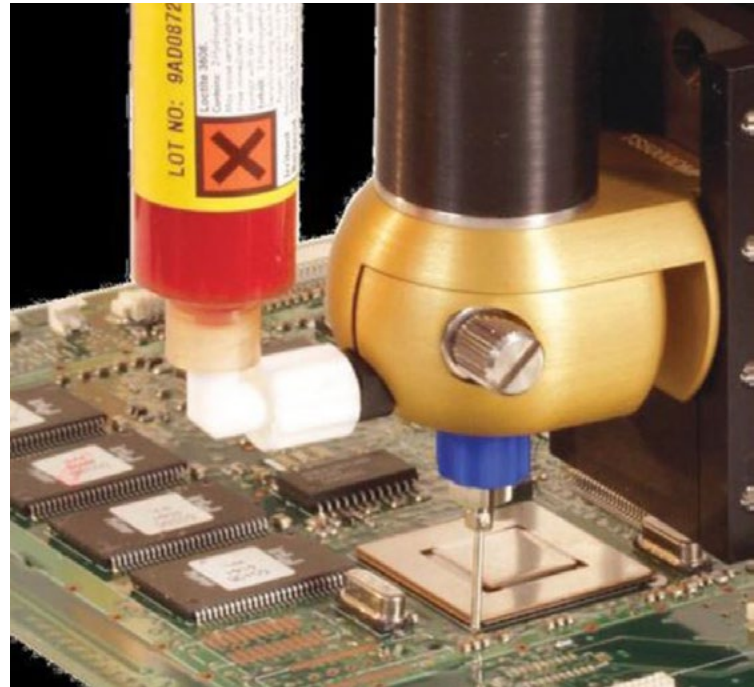


Figure 12: Dispensing epoxy underfill.

and the associated devices present on a PCB assembly, particularly in today's mobile devices. Attendees will understand the challenges inherent in each stage of the process and understand the need for process control to manage the risk of rework. A robust and repeatable rework process is essential for high rework yields. Proper preparation and application of solder and flux will add to the robustness and repeatability of the process. Reclamation of expensive components can be worthwhile if safely removed.

This article pays particular attention to the challenges associated with underfill epoxy and the lack of a robust, repeatable process and the need for a better solution for pad cleaning and preparation. Additionally, the industry lacks a reliable approach to removing epoxy from printed circuit boards which needs to be addressed. **SMT**



Paul Wood is the advanced product applications manager at OK International.



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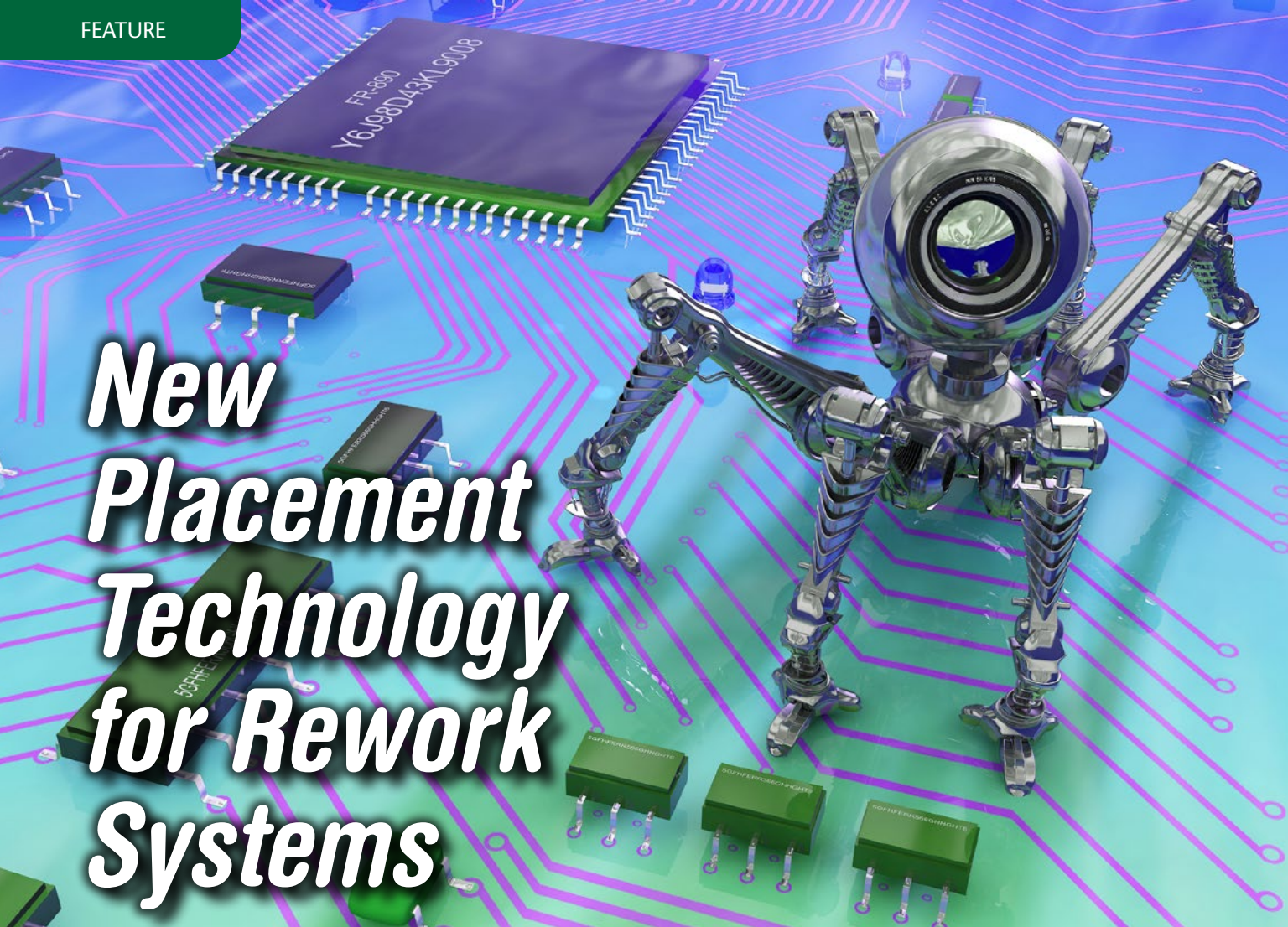
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# New Placement Technology for Rework Systems

by **Joerg Nolte**  
ERSA GMBH

## Abstract

In the fast developing electronic industry, the demands for production equipment are changing rapidly. The industry is looking for both stable production processes and automated procedures in order to have full control of quality and costs. This also affects the rework processes that are still commonly dependent on the knowledge and skills of operators who are handling repair and touch-up of electronic assemblies.

For a rework system to carry out automated user-independent rework, the placement process must operate automatically. A new placement technology uses two cameras to identify the target area for component installation and component pin structure. Image processing software calculates the correct placement posi-

tion for the component by using the image information. A motorized four-axis system is able to move the component to the target position without interaction of any operator. The procedure is based on an automatic pin detection algorithm along with a matching algorithm to find the correct position of the pin pattern in the target image. Several alignment procedures as well as camera corrections are implemented in order to reach the high demands of placement accuracy and repeatability.

The new placement technology relieves the user from exertive optical alignment and time-consuming manual adjustment as well as guaranteeing a high repeatability in the positioning results. While the system is placing and installing the component, the user can focus on preparative activities.

Besides automatic placement, the new rework technology allows automatic component flux and paste dipping as well as handling of paste printed components. Additionally solder-



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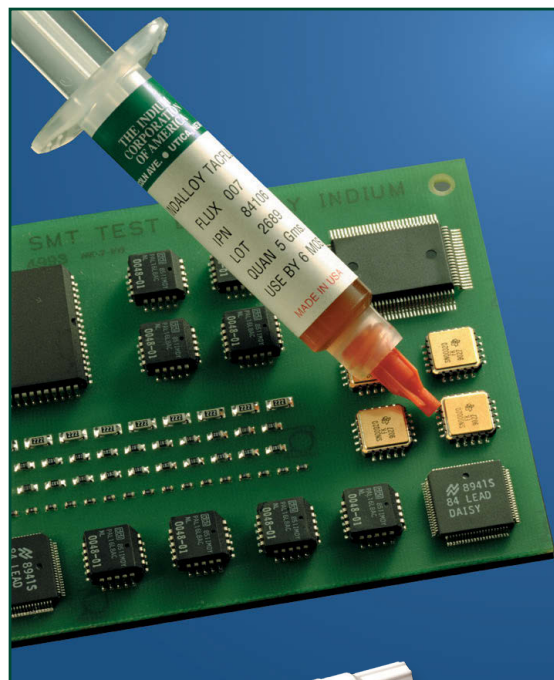
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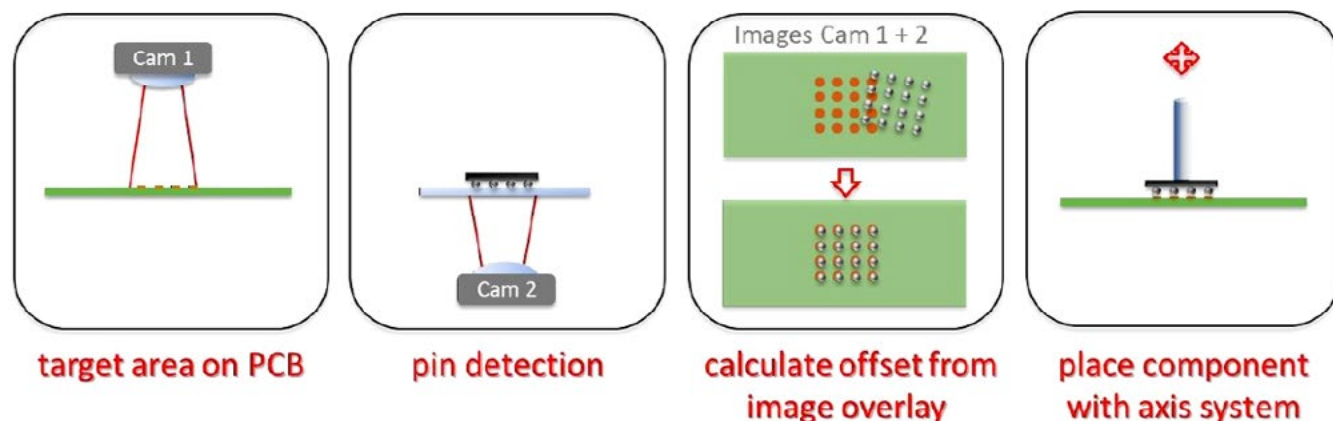


Figure 1: The component placement procedure, with two cameras generating images.

ing and desoldering processes are operated automatically.

### Introduction

Rework had a shadowy existence over the past 10 or 15 years. It was hard to accept that zero-failure production was, and currently is, a myth. But those in electronic production know that production failures have been present and will continue to exist. They have tried to get faulty assemblies to work, while others did not know how rework was accomplished and how the quality of the rework operators could ever be controlled.

With the SMT process standardized and widely understood, some experts have started to look closer at the side processes, including touch-up and repair of assemblies. Moreover, the introduction of bottom-terminated components, such as BGAs, has created a push for improved rework and repair activities. Another driver was the RoHS lead-free directive enacted in Europe in 2006, with formerly easy-to-handle rework activities struggling with smaller process windows and new materials. All in all, the responsible personnel recognized these challenges and requested more stable and repeatable rework equipment from the suppliers. A more detailed look at production costs led many customers to ask for better automated, fully controlled rework machines, prompting the development of new rework systems to satisfy such requirements. A detailed technical de-

scription of an example of this type of rework system follows.

### Current Technologies

The hot-air gun used for BGA repair has been declared obsolete by some in the industry, but in reality, they are still in the drawer. For more than 20 years, the suppliers of professional rework equipment have been presenting a battalion of different systems to remove and install bottom-terminated components and other SMDs. In the area of energy transmission for the soldering and desoldering processes, the territory was split up into “hot gas” and “infrared radiation,” but the means for component placement stayed the same. There was very little innovation in terms of alignment and placement of components onto the substrates.

The current component placement technologies can be divided into three major groups:

1. Placement with optical beam splitter
2. Placement with alignment tool
3. Vision placement

Other than in pick-and-place machines, during rework mostly only one component needs to be relocated onto a specific position on the PCB. CAD or Gerber data is often not available and most systems are not yet capable of handling such electronic information. In order to achieve a precise component handling and placement, all of these methods do require



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## NEW PLACEMENT TECHNOLOGY FOR REWORK SYSTEMS *continues*

an active operator. This is a disadvantage for at least two reasons: repeatability of component placement and the pure necessity to let an operator do the alignment.

### Placement with Optical Beam Splitter

Beam splitters allow operators to use one camera to visualize the PCB surface and component terminals in one image. This technology is commonly used, but reaches its limits in resolution and illumination as the pitch gets smaller and smaller. Aligning the component to its target position is a tiresome process for the operator if, for example, the color of component pins (bottom) and PCB pads (top) is the same.

### Placement with Alignment Tool

Another method involves use of a special tool that is aligned to the PCB pattern and later moves the desired electronic component onto the previously identified position. Due to a lack of magnification and possibly poor visibility, this technology is restricted to a certain number of package types. The quality of the alignment strongly depends on the user's abilities and skills.

### Vision Placement

Finally, the most promising method for component handling uses camera images and corner positions of the device and the target region. A computer-aided system calculates the offset and aligns virtual rectangular structures to each other. If the operator is identifying the

fiducial marks in high precision, the component placement will always be satisfactory. Some of the units providing this technology come with a high price tag and may not meet the cost expectations of many customers.

### A New Placement Technology

To combine and implement a new placement technology into a rework system with an acceptable market price is a challenging task. Digital cameras for image generation, image processing software and a precise gantry system are the baseline in order to establish this placement technology in the world of repair. USB cameras supply image information; image processing algorithms evaluate the data and do the necessary calculations to identify the correct position for a component. The stepper motor axis system is used to handle the device and locate it to the target position. Movements in x-, y- and z-directions are carried out with tolerances in the micrometer range and also the rotation of the component can precisely be executed.

### Digital Cameras and Image Processing

Crucial for a successful solution is the correct combination of the above-mentioned elements. The cameras need to generate images in acceptable resolution. Numerous algorithms must restructure the data, and the calculated pixel offset needs to be perfectly converted into steps and micrometers to match the component to its target position. For the cameras



Figure 2: A distorted image (left) and corrected image (right). (Source: MVTEC <sup>[1]</sup>)



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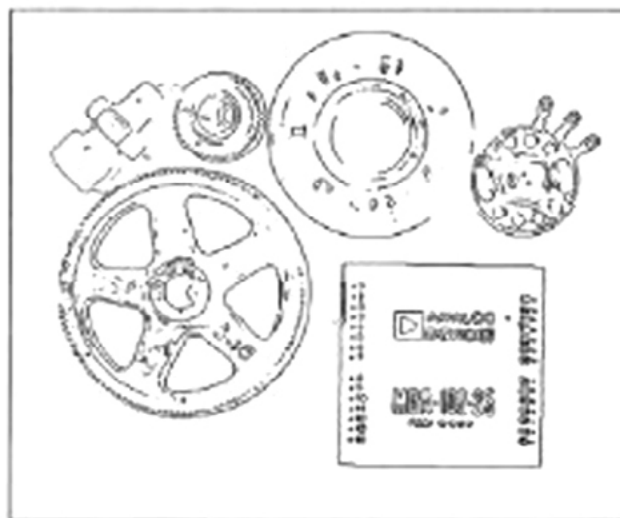


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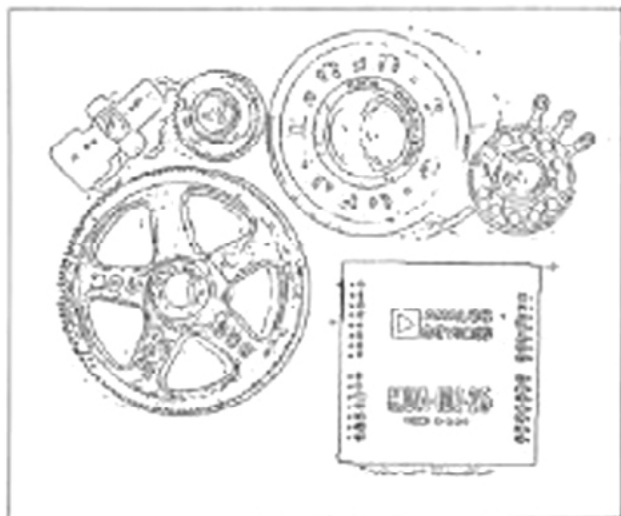


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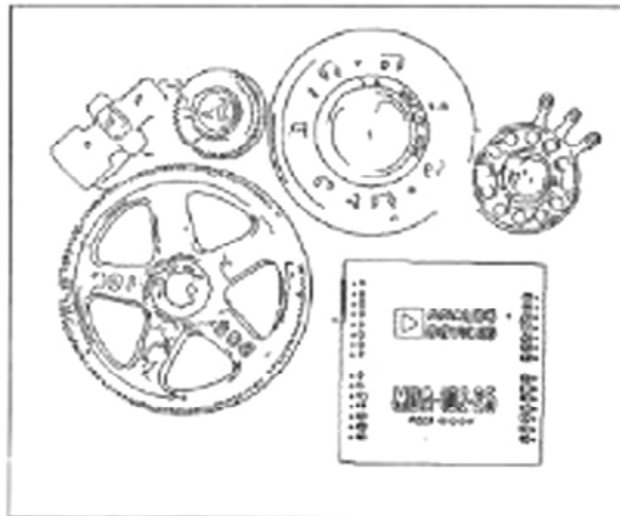
(a)



(c)



(b)



(d)

Figure 3: Parts image and Canny Edge Detector results with different thresholds. (Source: Wikipedia.org <sup>[2]</sup>)

and lenses, some corrections have to be implemented in order to attain one coordinate system for both cameras. Here the individual distortions of each camera and lens combination must be corrected prior to any further operation.

Another way to adjust the unit before any repair takes place is to calibrate the individual light conditions. As anyone can understand, an open unit with cameras on board is influenced by environmental light conditions, which can be recognized and calibrated. Extreme changes

in the surrounding light can be compensated and the built-in LED illumination is adapted to the new light situation. By doing this, the rework system can generate the best contrast images and precise placement in nearly any environment.

To find individual structures in images, like pins of a quad flat pack (QFP), a typical image processing procedure is "edge detection," a method developed by John Canny, an Australian scientist who developed the Canny Edge Detector algorithm in 1986.



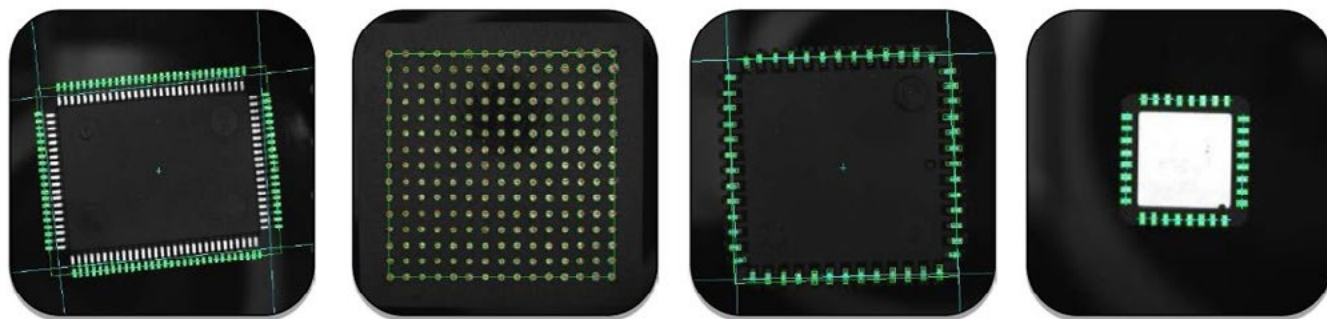
NEW PLACEMENT TECHNOLOGY FOR REWORK SYSTEMS *continues*

Figure 4 (left to right): Pin detection algorithm identifies terminals of QFP, BGA, PLCC and BTC QFNs components.

The computer is used to find changes of brightness in an image and interpret them as edges. Along with the information about the type of component being analyzed, the mathematics will identify, for example, regions in the images that represent the rectangular-shaped pins of a QFP component.

Some similar procedures have to be implemented to identify the pins of individual SMD components, such as BGAs, QFPs, BTC QFNs, and PLCC components. The benefit for the users is that they do not have to deal with any component-related data sets; they simply place the component onto a region above the camera and the software will find the pins of the component by itself.

When the component terminals are completely identified, the next objective is to find the pin pattern in the image of the PCB. A number of other mathematical calculations lead to a virtual overlay of the detected pin structure and the initially detected target area. The best result of this matching procedure can be presented to the operator for final approval or manual correction. The calculated offset between the current component location and the desired target position is used to place the part. In the automatic mode, the machine processes the entire sequence by itself.

In order to optimize the alignment accuracy for QFP components another algorithm is used to ideally match the pads and the pins. The pad row analysis compares the signals of the pad pattern and the pin pattern and readjusts the images until the best result has been detected.

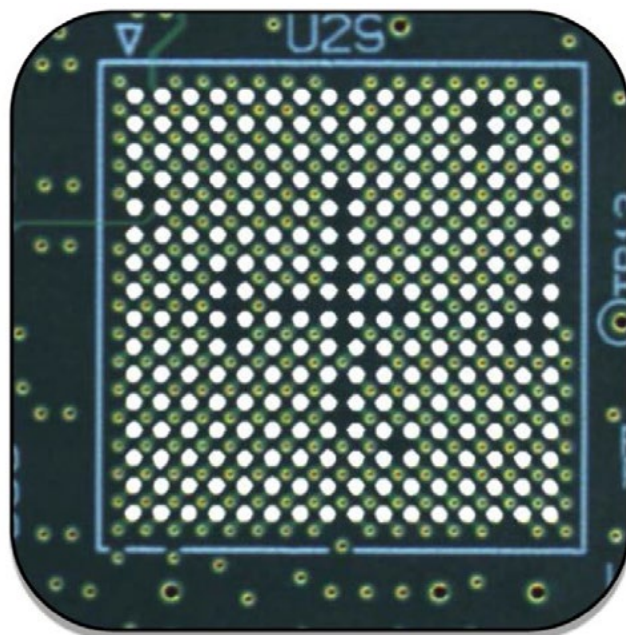


Figure 5: Target image with virtual pin overlay of the BGA component.

### Additional Benefits of the Gantry System

The matching result is usually calculated within some seconds and if the PCB to rework is only one out of a batch, the placement and following soldering procedure can be fully automated. In this case the gantry system will move the BGA to the target position, the heating head will move there in the next step and the preselected thermal process of soldering is begun.

As the rework machine is equipped with a precise gantry system, other beneficial aspects

## NEW PLACEMENT TECHNOLOGY FOR REWORK SYSTEMS *continues*

can be achieved with none to little additional effort: Treating more than one component automatically (for desoldering or placement and soldering) will be an easy task for such a system. Handling the component automatically and having cameras on board allows using the system for quality assurance aspects, by generating and evaluating images. For example, a component could be inspected if all pins are in order, before its treatment. It is possible to apply flux or solder paste onto the component with comparatively simple means in very precise portions, by the dipping method.

The dipping method requires the precision of the gantry system in combination with a precise cavity allows the supply of accurate and

small portions of solder paste to each individual solder ball (in the case of a BGA). The previously dipped component is aligned to the target position, placed and then is ready for soldering. The result of this rework process would be comparable to a soldering result created by a SMT production line.

### Outlook

As already mentioned, there will be obstacles in the way of this technology in terms of new and unknown components that cannot be handled by the system initially.

To address this question, there must be a deeper look into the methods of image processing. The key idea is to generate a learning system which will improve its own capability instead of being trained to new challenges by human programmers. Some questions may still demand answers, but if the human programmers concentrate on a learning system which is dealing with a flexible algorithm library instead of adapting a set of algorithms to new data, this vision might not be out of reach for the next generation of rework systems.

### Summary

Compared to the existing methods of component placement and treatment, this new placement technology implemented in a rework system opens up a field to repair complex electronic assemblies. At the same time, competitive cameras and stepper motor axes allow this technology to be available at a more widely accepted price level.

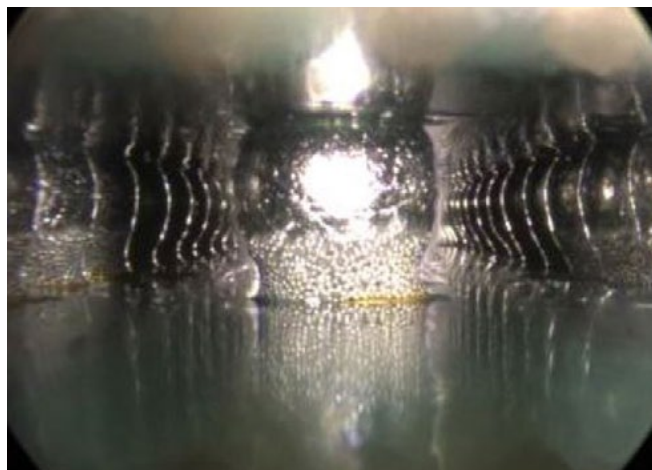


Figure 6: Side view image of a BGA ball, placed after the component was dipped into solder paste.

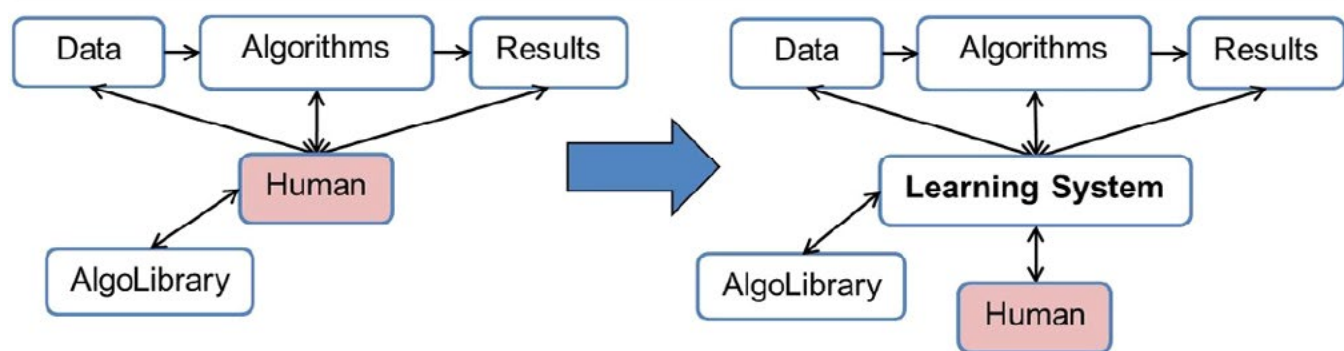


Figure 7: Method of learning system in image processing. (Source: Math & Tech Engineering GmbH <sup>[3]</sup>)



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Accuracy and repeatability of the procedures are increasing along with the higher degree of automation in the machine which can operate standard SMT components and bottom terminated components from 1 x 1 mm to 50 x 50 mm without any special tools for desoldering, soldering or placement. No component data needs to be supplied or evaluated; the operator can execute the rework process starting with the first assembly and the first component. The success rate can easily rise by more than 10% compared to simple, non-automated repair procedures.

Automated processes can save up to 30–50 % of the operator's time. The alignment of components is done by the rework system and the operator can concentrate on other activities with operator generated alignment mistakes removed reducing defects during rework. **SMT**

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Joerg Nolte is vice president for R&D rework, inspection and tools at ERSA GmbH.

## Physicists Find New Way to Push Electrons Around

When moving through a conductive material in an electric field, electrons tend to follow the path of least resistance--which runs in the direction of that field.

But now physicists at MIT and the University of Manchester have found that when a sheet of graphene is placed atop another two-dimensional material, electrons instead move sideways, perpendicular to the electric field.

What's more, two separate streams of electrons would flow in opposite directions, both crosswise to the field, canceling out each other's electrical charge to produce a "neutral, chargeless current," explains Leonid Levitov, an MIT professor of physics and a senior author of a paper describing these findings this week in the journal *Science*.

Levitov and co-author Andre Geim at Manchester say this flow could be altered by

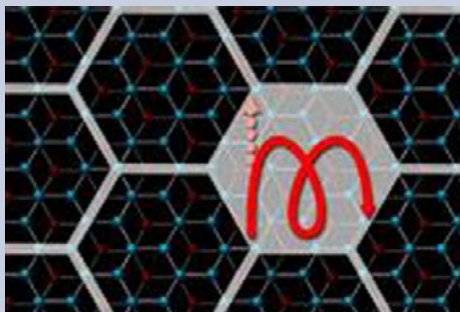
applying a minute voltage on the gate, allowing the material to function as a transistor.

"It is widely believed that new, unconventional approaches to information processing are key for the future of hardware," Levitov says. "This belief has been the driving force behind a number of important recent developments, in particular spintronics"--in which the spin of electrons, not their electric charge, carries information.

In their experiments, Levitov, Geim, and their colleagues overlaid the graphene on a layer of boron nitride--a two-dimensional material that forms a hexagonal lattice structure, as graphene does. Together, the two materials form a superlattice that behaves as a semiconductor.

Whether or not this effect can be harnessed to reduce the energy used by computer chips remains an open question, Levitov concedes.

The work has great potential, Guinea adds, because "two-dimensional materials with special topological properties are the basis of new technologies for the manipulation of quantum information."





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# Bare Board ECOs, ECNs and Design Modifications

by **Bob Wettermann**  
BEST INC.

## Abstract

While rework has been historically defined and memorialized by the IPC 7721 board-level repair guidelines as a populated board operation, there are many types of PCB ECOs on bare, unpopulated boards that require changing or modifying the physical aspects to the PCB. These cases are most commonly ones in which there has been an error in the board layout, a PCB fabrication error, or a design oversight. The most common types of physical board rework includes the adding or cutting of traces and pads, the select removal of solder mask, and the modification of board dimensions.

The types of physical rework that are performed most commonly on bare and populated PCBs, the most common options for reworking boards, and the methods used for performing this type of board-level rework will be discussed here. Case studies will be examined, along with photos of the board-level changes that were performed in order to evaluate the different methods.

One of the options for fixing a layout or design error, or to change the routing due to the use of other components, is to perform physical board modifications to populated and unpopulated PCBs. These ECNs or modifications need to be performed on the bare boards, keeping in



mind that subsequent board processing including stencil printing, reflow, wash cycle(s) and wave soldering will be performed on the PCB. In this case, both the “as built” board information and the “needs to be modified” board design information needs to be sent to the rework or remanufacturing location. Boards will then be shipped to the initial fabricator or rework services provider with a sample lot being shipped back as a first-article inspection prior to the remainder of the lot being modified. In some cases, boards can be simply respun so that





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**BARE BOARD ECOS, ECNS AND DESIGN MODIFICATIONS** *continues*

new bare boards arrive sooner than reworked ones, thus eliminating the need for board-level ECO/ECNs. Timing of these changes needs to be such that the supply pipeline does not have any discontinuity.

There are a variety of options available to the assembler or OEM for revising or fixing board errors. One of the options for fixing a layout, design or fabrication error, or to change the routing due to the use of another part configuration, is the respinning of a PCB. This involves the design or layout engineer revising the layout in the design software, redoing the output and re-sending the output files back to the PCB fabricator. It may take a couple of days to a couple of weeks to get the pipeline filled up again with new PCBs using this option.

In some cases a combination of both newly laid out, manufactured PCBs and modified boards that have been through the ECO/ECN process may be used. The ECO process may take place on the bare or populated boards. In order to keep the supply chain filled up, enough PCBs will need to be immediately modified while the process of changing the design, outputting newly revised Gerbers, manufacturing new boards, shipping and inspecting them, is completed. The start-to-finish time of getting newly manufactured boards back to the assembly operation may be several weeks. This timeline may be extended by several weeks if retesting of the new design is required.

A variety of different types of physical modifications may be required as part of the ECO/board modification stream on bare boards. The most common types of physical modification of PCBs include: conductor/trace/pad additions, conductor/trace cuts, selective solder mask removal, and physical board modifications such as the cutting of holes, the shaving of board outlines, or the creation of different physical geometries in order to get the board to properly fit/seat in a housing.

There are some cases in which conductive traces must be added to the visible surfaces of a PCB. There are also board modifications required in which test points or additional pads are added to the layout. This is very straightforward when the trace or pad can be made or modified from an underlying ground layer and the solder mask can be selectively removed from the PCB (Figures 1 and 2). In other cases, one or more traces must be added in areas where there is not an underlying electrical connection to the first ground layer, or when there are many conductive runs which need to be added.

Besides adding traces, in some cases errant signals are being picked up from traces in addition to incorrect connections between two conductors on the board. In these scenarios, a conductor run or runs must be severed and properly insulated (Figure 3).

In some cases, solder mask needs to be selectively removed in order to gain the proper

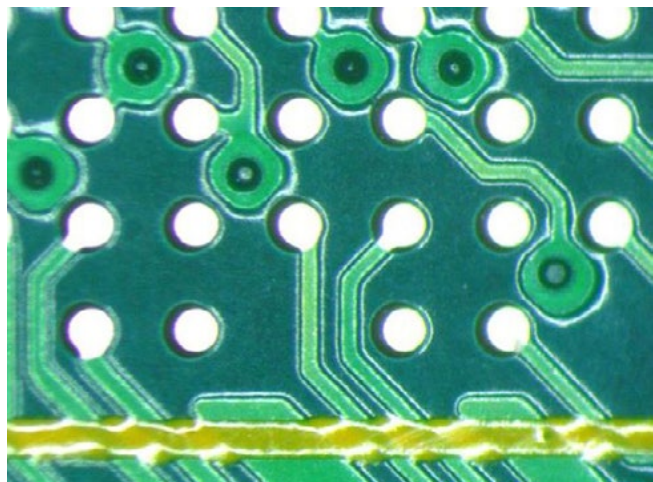


Figure 1: Initial area of the board requiring both trace additions and circuit trace cuts.

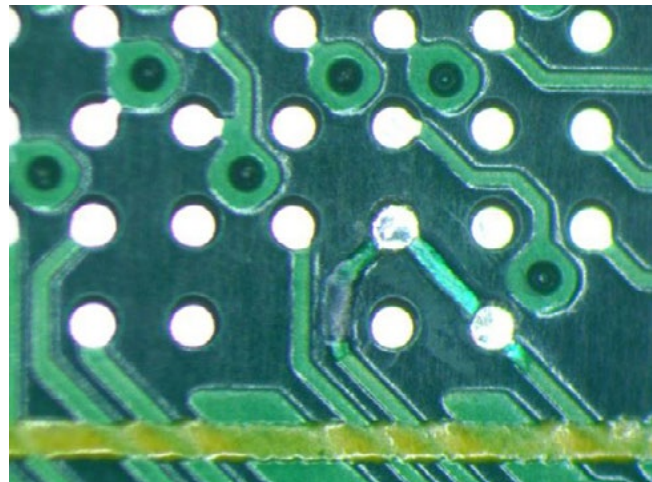


Figure 2: After modification where both a trace has been cut and another one added.



pad geometry. Or in some situations, the proper “fit up” for a shield or ground pattern for the component must be made. In these cases, solder mask needs to be selectively removed (Figures 4 and 5).

A final grouping of this type of board modifications involves modifying the physical dimensions of the PCB. Modifications which may be required include changing the physical outline of the board, adding holes in select areas of the PCB in order to mount it, and shaving a few tenths of a millimeter from the PCB in order to fit it properly into the enclosure or housing.

### Methods for Physical Board ECO/ECNs and Modifications

For each of the different physical modifications, including the addition of trace and pads, the cutting of conductors, the selective removal of solder mask and the physical modification of PCBs, numerous other methods are commonly employed to make these changes.

A variety of processes can allow traces to be added while still permitting processing and assembly a PCB. What is critical is making sure the addition can withstand squeegee pressures and that the trace is not negatively impacted by subsequent reflow temperatures. One of the methods, if the layout of the top layer of the PCB allows, relies on a solid-state laser to selectively ablate the solder mask in a given area. A second method relies on either the IPC-7721 Method 4.2.1. (epoxy method) or 4.2.2. (dry film method) for the adherence of a new conductor by way of a replacement circuit frame.

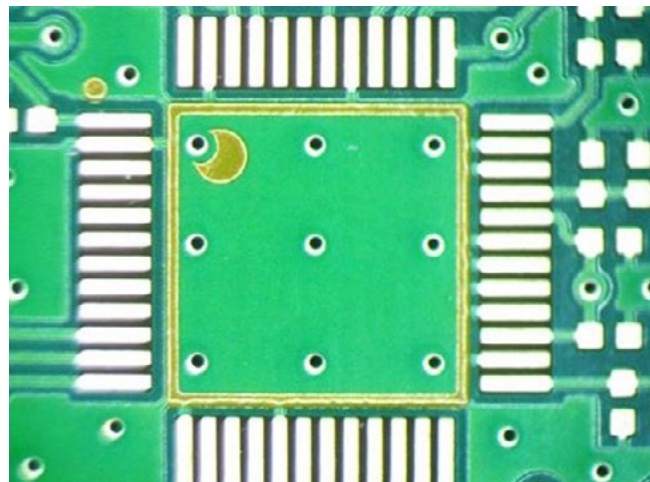


Figure 4: QFN ground plane prior to solder mask ablation.

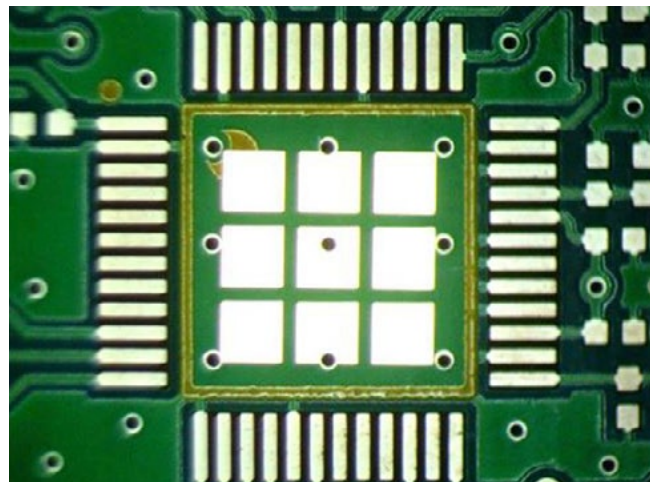


Figure 5: QFN ground plane after solder mask ablation.

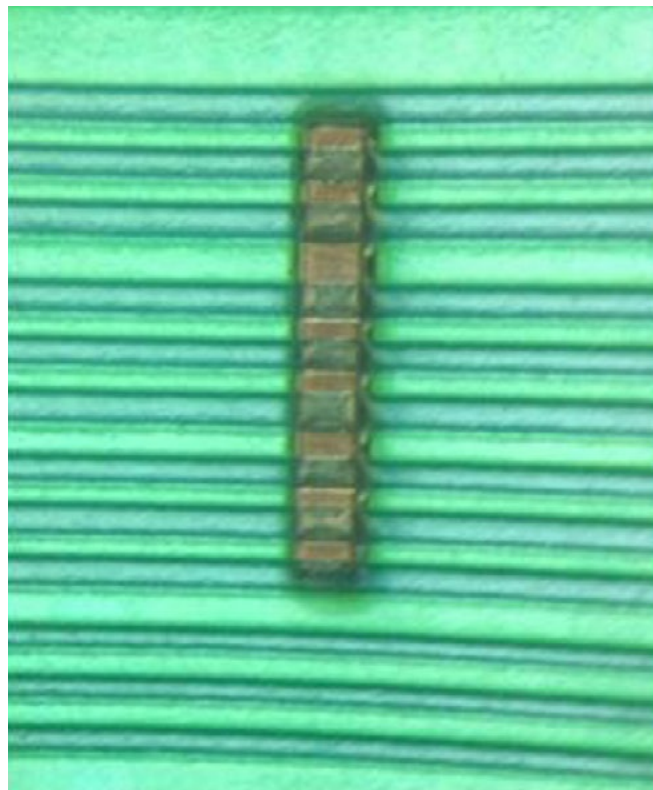


Figure 3: Trace cuts on several signal lines need to be precisely cut (3 mils spaces and traces).

**BARE BOARD ECOS, ECNS AND DESIGN MODIFICATIONS** *continues*

These methods are manual in nature and are very time-consuming and therefore expensive to perform in high labor-cost countries.

A final method relies on a complete circuit frame which is adhered with a specialty epoxy. In this method, all of the replacement traces and pads are adhered to the PCB surface at one time using a replacement copper frame. This makes it a good choice for higher-volume, more complicated repairs, as much of the highly skilled labor element is taken out of the process. These replacement frames are aligned with the board fiducials in a semi-automated process. After being custom fabricated for the additions of the lands and pads required, the surface of the replacement copper pattern is adhered with B-stage adhesive. Finally, heat and pressure in this lamination process allow the “sandwich” to be adhered to the PCB.

**Pad Additions**

A variety of processes allow for PCBs to have pads added, much like traces, without affecting processing and assembly. One of the methods, if the configuration of the change allows, relies on a solid-state laser to selectively ablate the solder mask in a given area to fabricate or modify a pad location. A second method, like that of the trace modifications, is found in the IPC-7721 Method 4.5.1. (epoxy method) and 4.5.2. (dry film method) for the adherence of a new pad through a replacement circuit frame. As previously stated, these methods are manual in nature and are very time-consuming and costly on a mass basis, even with customized frame patterns. The final method relies on a complete circuit frame which is adhered with a B-stage epoxy. In this method all of the replacement traces and pads are adhered to the PCB surface at one time making it a good choice for higher volume more complicated repair. Both pads and traces are routinely added using one of the aforementioned techniques.

**Conductor/Trace Cuts**

There are several manual and machine-based conductor cutting techniques which can be used to modify either populated or non-populated PCBs. The most common manual methods which are used include the breaking

of a conductor run by either hand-scribing with a Dremel, scraping with a sharp dental tool, or small sharp knife (IPC-7721 4.1.3). In these methods, the cut is made by severing the trace. This is followed by gluing down any part of the trace which has been lifted in the cutting process and making sure that an electrical open (high resistance) has been created in the process. The cut must be at least as wide as the minimum conductor width. The area is then sealed with epoxy by confirming there is an insulator in the area where the circuit was cut. Alternately, a small ball end mill can be placed in a Dremel tool and can be used to rout an area where the conductor needs to be severed. A galvo depth-controlled laser can alternatively cut very precisely (line width of a few microns) the copper trace material without cutting down in to the laminate. Finally, precision mills as seen in Figure 6 can also be used for depth controlled trace cuts.

**Selective Solder Mask Removal**

For selective solder mask removal there are several techniques that can be employed. For manual solder mask removal a Dremel tool with a ball end mill (IPC-7721-2.3.5); a dental scraper (IPC-7721-2.3.5), as seen in Figure 7; and a microblaster (IPC-7721-2.3.6), as shown in Figure 8, can be used to ablate the solder mask from selective areas. For each of these methods extreme care must be taken in order to not damage nearby components or the PCB laminate.

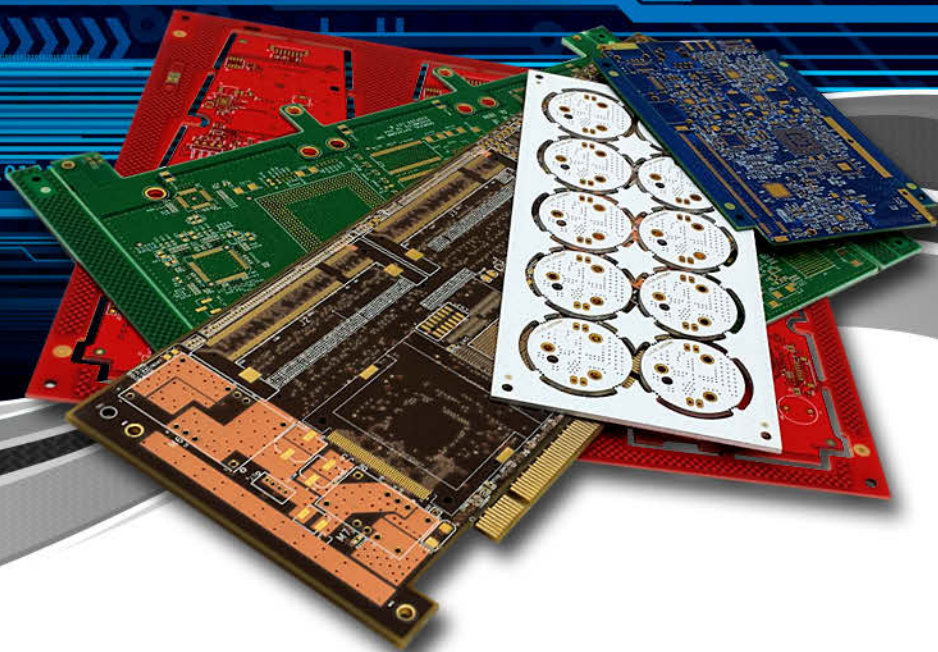


Figure 6: High-speed routing system in action. (Courtesy LPKF)



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**BARE BOARD ECOS, ECNS AND DESIGN MODIFICATIONS** *continues*

Figure 7: Manual mask ablation tool.



Figure 8: Micro ablation of solder mask.

Because these are manual processes, board-to-board consistency is hard to maintain.

For the microblasting system, corn starch, nut shells and other specialty abrasion materials can be used to selectively remove solder mask. Care needs to be taken to make sure that excessive material is not ablated, nor are excessive ESD charges generated, which can harm components. If the bare boards will be in storage for a long period of time, then OSP or another protective coating should be applied to the exposed copper in order to protect its solderability until being populated. Ultrafine patterns with accuracies to 1 mil (.0254 mm) can be ablated with the use of a galvo-controlled laser source. Solder mask applied directly onto an FR-4 surface and not directly over a ground plane requires use of a depth-controlled laser in order to remove the solder mask without damaging the board. Laser mask ablation is designed for high-precision, high-volume requirements as it is a highly repeatable, fast process.

### Physical Board Modifications

There are a variety of methods for modifying the physical dimensions of a PCB. High-speed, high-precision numerically controlled milling

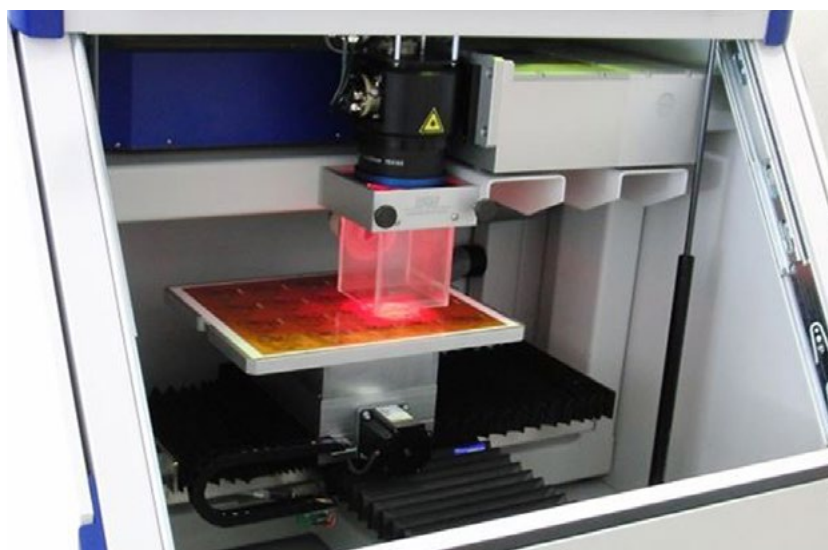


Figure 9: Laser cutting and scribing example. (Courtesy LPKF)

machines and lasers are the most commonly-used tools in order to make these modifications on both populated and unpopulated boards. When using high-speed milling machines, it is critical to use the proper board fixturing because excessive vibration can cause solder joint cracking as well as excessive mechanical stresses on the PCB. An example of such an engineering change would be the addition of a mounting hole in a PCB. Laser cutting of the PCB brings a high-precision method for shaving off a few thousandths of an inch as well being able to cut difficult routing shapes and



**BARE BOARD ECOS, ECNS AND DESIGN MODIFICATIONS** *continues*

patterns. Both of these methods are employed when the physical dimensions or mounting hole patterns need to be changed on a PCB.

### Conclusion

There are a variety of PCB fixes which may need be made to the physical PCB due to errors in the board layout, part changes or PCB board fab errors. There are a variety of options available, including but not limited to board respins, scrapping of the boards, and reworking the boards, whether they are already populated or not. The most common fixes to these errors include cutting of the conductors, selective solder mask removal, addition of traces and pads or mechanical routing or drilling of holes. A variety of proven industry methods, depending on the type of fix required, are available to make these adjustments. **SMT**

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3. "Laser – A flexible tool for PCB and device rework," Wettermann, Robert. SMTAI August 2008.

4. "PCB Pad Site Dress Methods on BGA and Socket Pad Arrays," James Wade and Raiyo Aspandiar; Don Naugler and Terry Leahy, IPC APEX EXPO 2010.



Bob Wettermann is the quality manager of BEST Inc. and an MIT. He is the author of numerous articles and has presented at a variety of SMTA, ASQC, IPC and other international conferences on the topic of PCB rework, repair and assembly.

## Video Interview

### Alternative Methodologies for High-Temp Bonds

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Tim Jensen, senior product manager with Indium, discusses some of the newer lead-free solder alternatives that are suitable for high-temperature (and low-temperature) applications.



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# **SMOnline Supplier/New Product News Highlights**



## **Panasonic Introduces NPM-D3 to SMT Platform**

"The NPM-D3 brings the industry's first, single-unit camera for alignment, thickness, and coplanarity," said Mark Ragard, GM, Electronics Assembly Sales. "Beyond 3D multi-recognition, the NPM-D3 offers board warp detection, adaptive process control, and auto board support pin—features that contribute to lean assembly, maximum productivity, and impressive investment protection."

## **Intertronics Intros New DYMAX Encompass Technology**

Intertronics has launched new DYMAX Encompass technology in a range of light-cure adhesives, which combine the benefits of colour change once cured with red fluorescence. This combination offers the significant improvements in production efficiencies gained from rapid, on-demand curing while ensuring greatly improved quality outcomes.

## **Alpha Releases TrueHeight Spacer Blocks**

Named for their precise height control and burr-free edges, these non-collapse disc spacers from Alpha mitigate corner solder bridging caused by BGA warping during SMT reflow. The spacer blocks are offered in tape and reel packaging for automatic placement with excellent pick rate yield.

## **SMTA Recognizes Indium with Corporate Award**

Indium Corporation was presented with SMTA's Corporate Award on Tuesday, September 30, at the Members of Distinction Awards Ceremony at SMTA International in Rosemont, Illinois. This award is not based on a product or a process, but rather on company's contribution to the overall success of SMTA.

## **Digitaltest Added to Panasonic's PanaCIM Program**

Panasonic Factory Solutions Company of America has announced the addition of Digitaltest solutions and equipment to the PanaCIM Certified Technology Program.

## **EasyBraid Partners with Allied Electronics**

John Webber, National Sales manager, stated, "This new partnering with Allied significantly benefits customers here in the U.S., Canada, and Mexico. The products EasyBraid provides enhances Allied's ability to find solutions for their customers' needs with our 400+ products in the PCB assembly industry."

## **R.H. Technologies Installs Two New Mek AOI Systems**

Marantz Business Electronics (Mek), recently announced the installation of its tenth and eleventh AOI system at RH Technologies. The Israel-headquartered EMS provider recently commissioned two new PowerSpector FDAz in-line AOI systems, complementing the existing nine Mek systems.

## **Douglas Electrical Components Earns IPC 620 Certification**

The IPC-A-620 program is the only industry quality assurance standard for cable and wire harness fabrication and installation agreed upon by members of the IPC and the Wire Harness Manufacturers' Association.

## **Firstronic's Juarez, Mexico Facility Begins Production**

The company's new facility in Juarez, Mexico, began production qualification runs this month. Facility preparation was completed earlier in September and the first two SMT lines have been installed. The facility is only five minutes away from the Mexican border across from El Paso, Texas, providing the cost advantages of Mexico and the logistics simplicity of the border crossing.

## **Firstronic Wins Global Trader of the Year Award**

Firstronic LLC was named Global Trader of the Year at the 14th Annual Automation Alley Awards Gala held September 12 at the Motor City Casino Hotel in Detroit, Michigan. Automation Alley's Annual Awards Gala honors technology organizations and their leaders.



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# Avionics: Atmospheric Pressure Plasma Case Study

by **Inès A. Melamies**,  
BLUE RONDO INTERNATIONAL AND  
**Tim Smith**, PLASMATREAT NORTH AMERICA

The aviation industry's requirements regarding the integrity and service life of safety-relevant components far outweigh those of other industries. Due to its virtually zero potential, an atmospheric pressure plasma process secures not only the adhesion of the conformal coating of SMD-boards in aircraft radio communication, but does so without any damage of the highly sensitive electronic components.

According to the International Civil Aviation Organization (ICAO) some 3.1 billion passengers made use of the global civilian air transport network in 2013<sup>[1]</sup> and have thus relied on the quality and reliability of air traffic control systems. The main task of air traffic controllers is to guide aircraft on the ground and in the air by radio to prevent collisions. Passenger safety depends to a large extent on clear communication between air traffic controllers and pilots, and relies on the correct functioning of electronic aircraft radio systems.

Crews on long haul flights use shortwave radios to communicate with air traffic control, and to stay in touch with their airlines from anywhere in the world. These devices allow uninterrupted communication even on routes over the poles where satellite networks cannot be used.

Rohde & Schwarz, a manufacturer of wireless communications and EMC test and measurement equipment, and broadcasting and T&M equipment for digital terrestrial television, also

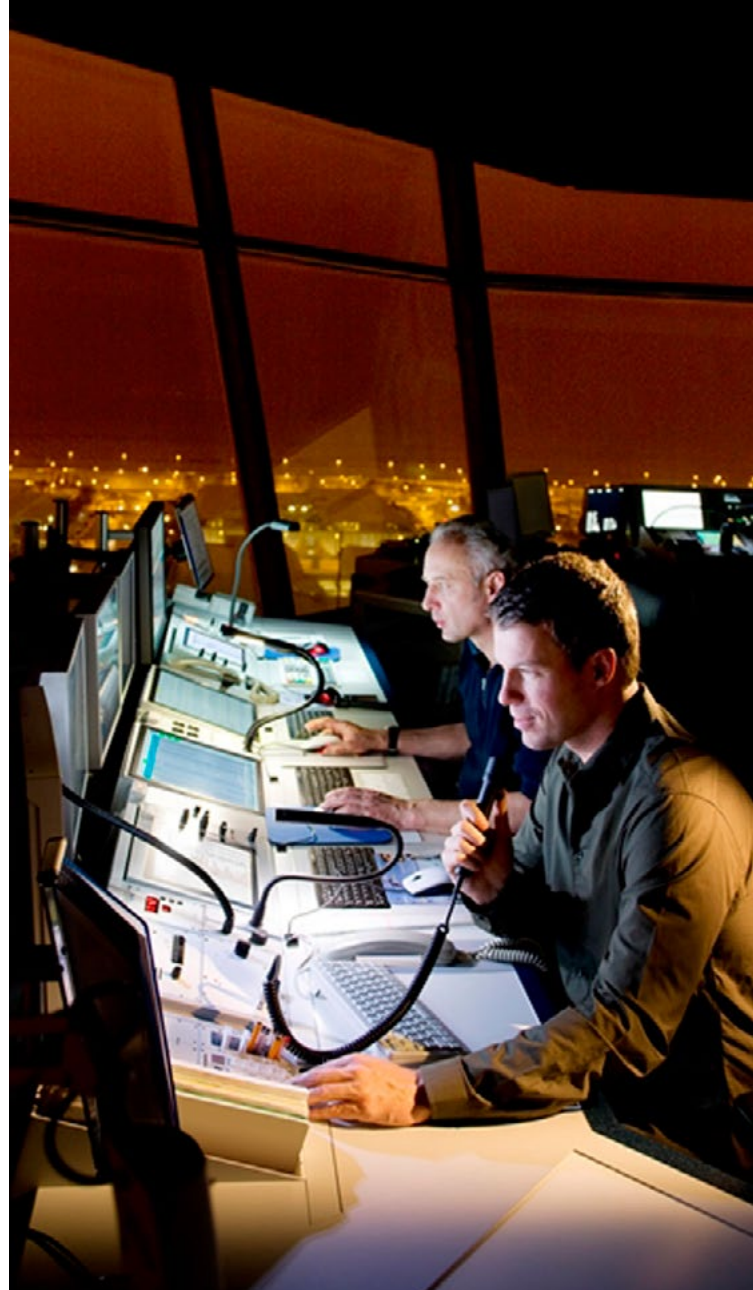


Figure 1: The safety of billions of air travelers depends on uninterrupted radio communication between air traffic controllers and pilots. (Photo: Rohde & Schwarz)

manufactures these airborne radios, which are required to meet the highest safety standards. These high-tech systems are produced by the subsidiary Rohde & Schwarz Messgerätebau GmbH, which is responsible for assembly, final testing and shipping of almost all the company's products. Barely a single long-haul aircraft in the world lands or takes off without the assistance of an XK/FK 516 shortwave radio produced by this specialized Bavarian company. At the core of the FK 516 antenna tuner developed



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**AVIONICS: ATMOSPHERIC PRESSURE PLASMA CASE STUDY** *continues*

specifically for civilian airborne radio communication and long-haul flights is the tuning control unit: a circuit board fitted with several hundred tiny plastic-coated SMDs (surface-mounted devices). The function of this SMD assembly is to reliably tune the antennae, thereby ensuring overall radio communications.

**Unexpected Adhesive Problem**

Conformal coating came to an abrupt end one day when it was discovered that the transparent protective coating had lifted on around 50 transistors. Since nothing whatsoever had changed in the assembly, pre-cleaning or coating process, it became apparent that the root of the problem could only lie with the component material itself. And sure enough, when questioned, the supplier confirmed that it had changed the composition of its plastic blend. This is a problem frequently encountered by processing companies that are reliant on plastic components produced externally since even the slightest alteration to the composition can be enough to totally change the surface characteristics of the material. This news from the supplier was alarming, because there was no alternative to the new plastic blend. There was simply no other certified manufacturer available who could produce these particular electronic components.

"We had to find a solution as quickly as possible to ensure the adhesion of the conformal coating," explains Michael A. Schneider, mechatronics engineer in charge of production technology at Rohde & Schwarz. "Without a reliable adhesive bond it would no longer be feasible to continue manufacturing the tuning control units."

**Surface Activation**

As is well known, materials are made more receptive to adhesion by means of activation; in other words, by pretreating them so as to increase their surface energy. This is the most important measure for determining the probable adhesion of an adhesive layer or coating. Reliable, long-time stable adhesion is conditional on the material surface being ultra-clean and the surface energy of the solid material being higher than the surface tension of the liquid—in this

case the coating. Various pretreatments are available to achieve these two conditions, with wet chemical substances still the most widely used.

**Difficult Choice**

But finding the right pretreatment for these highly sensitive electronic components seemed almost impossible at first. Schneider: "Activation using a solvent-based primer was not an option for us. Partly because these substances are extremely harmful to the environment and partly because they would incur enormous costs in terms of health and safety (e.g., explosion protection) and disposal." The electronic engineers also ruled out laser pretreatment on the grounds that the uneven surface of the material would have made the coupling efficiency unpredictable. CO<sub>2</sub> snow blasting, which cleans but has no activation capability, was also rejected. The final method under consideration was a low-pressure plasma treatment; a highly effective activation process, but not suitable for this purpose because the vacuum would have drawn the fluid out of the wet electrolytic capacitors contained in the SMD assembly. "We seemed to be very far from finding a way around this



Figure 2: Avionics specialist Michael Schneider (left) and plasma expert Peter Langhof (right) standing in front of the Openair-Plasma system. (Photo: Plasmatreat)



**AVIONICS: ATMOSPHERIC PRESSURE PLASMA CASE STUDY** *continues*

problem,” recalled the engineer, “but then I stumbled across a solution at an automation trade fair. This is where I discovered atmospheric pressure plasma.”

**The Solution**

The pretreatment process developed and patented under this brand name by Plasmatrete GmbH in the mid-90s is now used throughout the world in almost every branch of industry. The environmentally friendly in-line technology works under normal ambient air conditions, thereby dispensing with the need for a vacuum chamber.

The plasma process performs two operations in a single step: It simultaneously brings about the microfine cleaning and strong activation of the plastic surface. The rise in temperature of the plastic surface during plasma treatment is

typically less than 30°C and substrates can be transported through the plasma jet at speeds of several hundred meters per minute. For electronic components, patented rotational nozzles with a special gentle action are used.

Schneider was soon convinced of plasma's powers of activation, but now the manufacturing specialist had to face a complete different question: Would the sensitive electronics survive the plasma treatment unscathed?

It was clear from the very first tests performed on a plasma system supplied on loan that this plasma technique had not damaged the electronics. The surface energy of the plastic transistors which had caused the whole problem increased from below 30 dyne in the inactivated state to over 70 dyne following plasma treatment. The final visual UV inspection, which every SMD component undergoes before

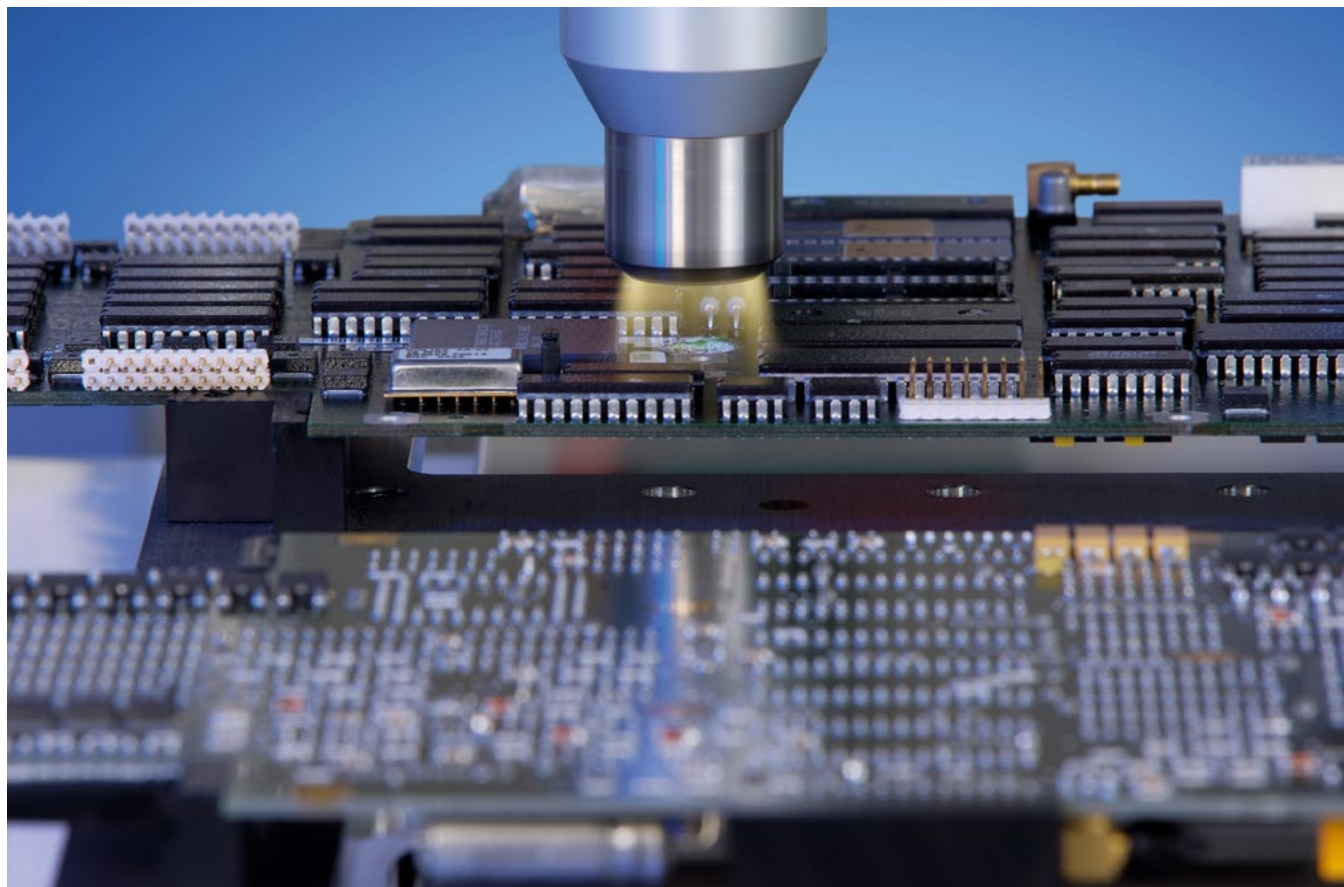


Figure 3: The smoothly working rotary plasma jet cleans and simultaneously activates the surface of the plastic components just before conformal coating. The pretreatment is done in a matter of seconds without damaging the sensitive electronics. (Photo: Plasmatrete)

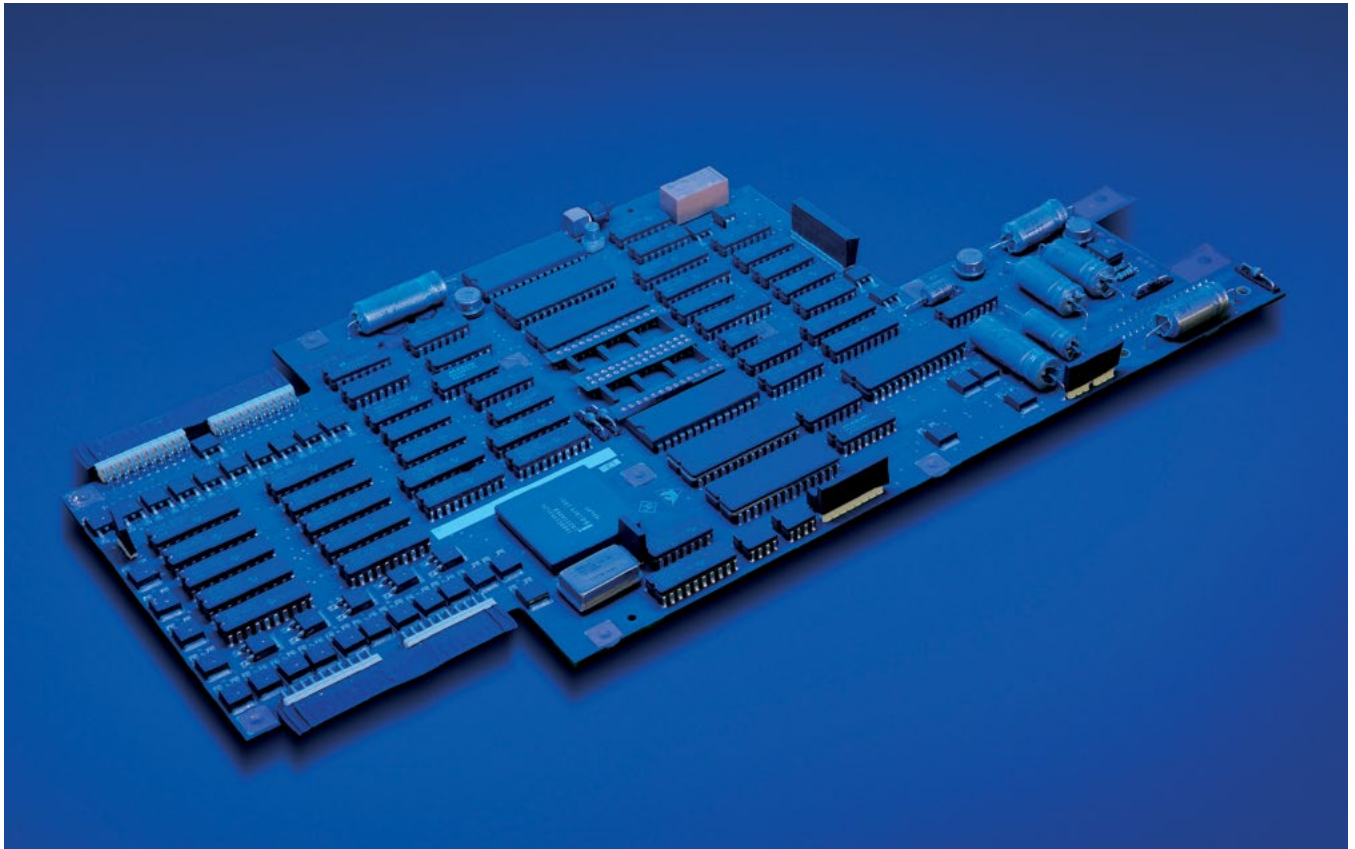
**AVIONICS: ATMOSPHERIC PRESSURE PLASMA CASE STUDY** *continues*

Figure 4: The coating's adhesive bond is visually inspected under UV light before the SMD assembly is mounted in the radio. Then a burn-in test is performed to verify its stability (Photo: Plasmatreat).

assembly, also showed that there was not a single area where the coating had lifted.

**Endurance Test**

The aviation industry's requirements regarding the integrity and service life of safety-relevant components far outweighs those of the automotive industry, whose requirements are themselves recognized as being very tough. One example of this is the burn-in test that is performed post-production on tuning controls. To understand the rationale behind this test it's helpful to know that airborne radios are rarely installed in the plane's air-conditioned and pressurized engine area. Mostly they are located in the nose of the aircraft where very different temperature and humidity conditions prevail. This is why it is so important to ensure that the protective coating is fully bonded to the electrical components.

Even the smallest leak would result in moisture ingress, potentially leading to complete failure of the radio communications system. What most air passengers don't realize is that all passenger planes are obliged to carry two sets of radio equipment on board; the second as backup in case the first one fails. If a plane lands at its destination with a defective radio system, it has to stay on ground until a spare radio set has been acquired and fitted.

The purpose of the burn-in test is to investigate continuous operation and accelerated ageing of electronic components. As the toughest load test available for electronic circuit boards, it is used to detect manufacturing faults which were not picked up earlier and to identify components that would fail in continuous operation. Burn-in is performed on the finished radios under operating conditions (i.e., powered up and with antennae). The test consists of a series





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## AVIONICS: ATMOSPHERIC PRESSURE PLASMA CASE STUDY *continues*



Figure 5: The XK/FK 516 shortwave radio guarantees airborne communications. The FK 516 antenna tuning unit with built-in tuning control (left); the matching amplifier (right). (Photo: Rohde & Schwarz)

of eight-hour cooling and heating cycles; after a four-hour cooling cycle at  $-55^{\circ}\text{C}$ , the temperature in the burn-in chamber is pushed up to  $+70^{\circ}\text{C}$  in a matter of a few minutes and held for a further four hours before plunging back down equally rapidly to start the next cooling cycle.

These cooling/heating cycles are repeated nine times, amounting to three days. During this time the radio system experiences a non-stop exposure to rapid and extreme temperature variations (Figure 5). If the plasma had damaged the electronics, the components would eventually have failed during this test. It would equally have become apparent if the coating's adhesion to the plastic would have not been sufficient.

### Summary

Test results were conclusive: The electronics functioned perfectly and the coating adhesion was long-time stable. Schneider said, "This plas-

ma technology reduced the number of process steps and enhanced the quality of our product within a very short space of time." **SMT**

### References:

1. ICAO 2013 Air Transport Results.



Inès A. Melamies is a journalist based in Germany who has written extensively on atmospheric plasma-jet technology.



Tim Smith is vice president of engineering and operations of Plasmatreat North America and director of the Canadian Technology Center in Ancaster, Ontario. For more information, contact

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# SMTonline Market News Highlights



## **Conference Board Consumer Confidence Index Drops**

The Conference Board Consumer Confidence Index®, which had increased in August, declined in September. The Index now stands at 86.0 (1985=100), down from 93.4 in August. The Present Situation Index decreased to 89.4 from 93.9, while the Expectations Index dropped to 83.7, from 93.1 in August.

## **Internet of Things Market to Reach \$1423B by 2020**

The value of Internet of Things market is expected to reach \$1423.09 billion by 2020, at an estimated CAGR of 4.08% from 2014 to 2020, whereas the Internet of Nano Things (IoNT) Market is forecast to be worth \$9.69 billion by 2020.

## **3D Printing Market Forecast to Reach \$8.6B by 2020**

North America leads the 3D printing market with approximately 43.9% revenue share in 2013, followed closely by the European region. The dominance of the North American market is attributed to growth in the healthcare, consumer, aerospace, and automobile industries.

## **Big Data Technology, Services to Reach \$41.5B in 2018**

International Data Corporation (IDC) forecasts that the Big Data technology and services market will grow at a 26.4% compound annual growth rate (CAGR) to \$41.5 billion through 2018, or about six times the growth rate of the overall information technology market.

## **Medtech Market to See Sales of \$514B by 2020**

"This is a year of change for the medical device market, particularly within the cardiology and orthopaedic spaces, which have been dominated by megamergers," said Ian Strickland, report author. "If the deal between Covidien and Medtronic goes through, we could see a new market leader. In an industry forecast to be worth more than half a trillion dollars in 2020, that is no insignificant achievement."

## **Personal & Domestic Robots Sales Continue to Soar**

Sales of medical robots decreased slightly by 2% compared to 2012, to almost 1,300 units in 2013, accounting for a share of 6% of the total unit sales of professional service robots. The most important applications are robot assisted surgery and therapy with more than 1,000 units sold in 2013, 2% less than in 2012.

## **Medical Electronics Market to be Worth \$56.5B by 2020**

An increase in lifestyle diseases continuously pushes patients for medical monitoring to get their health status to avoid any health related contingencies; medical devices such as cardiac monitors and hemodynamic monitors are continuously gaining market share in the medical monitoring applications.

## **Wearable Electronics Market at \$11.61B by 2020**

The global wearable electronics products market revenue is expected to grow roughly at a CAGR of 24.56% and cross \$11.61 billion by the end of 2020, with steady sales of wristwear and footwear category, along with the emergence of the small market size for eyewear and bodywear category.

## **Wearable Device Shipments to Quadruple by 2017**

New findings from Juniper Research have revealed that global smart wearable device shipments will more than quadruple by 2017, reaching 116 million units, compared to an estimated 27 million this year. However, this still suggests that less than 5% of smartphones will be used with such wearables by this time.

## **U.S. Small Businesses Segment Continues Decline**

According to D&B's proprietary data, the small businesses segment continues to decline as segments expected to ignite growth, flounder. "While overall business health across the country remains virtually unchanged, small businesses continue to experience inconsistent growth patterns," said Paul Ballew, chief data & analytics officer.



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# High-Reliability, Pb-free, Halogen-free Solder

by **Ian J. Wilding & Gavin J. Jackson**  
HENKEL LTD, UNITED KINGDOM

## Abstract

With increasing demand for the use of Pb-free solder materials coupled with an increasing requirement for halogen-free solder paste formulations, some market sectors are experiencing several challenges using standard SnAgCu (SAC) halide-free solder materials, especially in electronic assemblies for automotive products experiencing harsh operating environments such as high operating temperatures, increased thermal cycling conditions, high levels of vibration and contact with liquids such as moisture and lubricants. For example, in automotive 'under the hood' conditions, temperatures easily exceed 125°C and can cycle lower than -20°C. The reliability required to survive these harsh conditions is often greater than standard SAC solders can provide. In this paper, the performance of a specifically designed Pb-free solder alloy for increased reliability in high temperature thermal cycling is discussed.

Reliability can also be impacted by no-clean post reflow residues adjacent to solder joints.

These may potentially interact with other surface materials causing corrosion issues or lower insulation resistance. With halogen-free electronic assemblies arguably becoming more favourable than halide-free—even within some automotive manufacturers—solder paste manufacturers are now faced with the challenge of formulating halogen-free fluxes which can also demonstrate high reliability. While removing the halogen from a material is not difficult, replacing it with an activator set that can deliver a wide reflow process window whilst retaining or increasing reliability is a significant challenge. The paper also documents the challenges and breakthroughs in developing halogen-free or zero-halogen solder fluxes that are compatible with the Pb-free alloy specifically designed for higher reliability.

## Introduction

Reliability testing of standard SAC-based alloys as a direct comparison to Pb-containing materials as a response to the implementation of the RoHS directive during the mid-2000s has been well documented<sup>[1,2,3]</sup>. The results of the testing broadly concluded that little differences





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**HIGH-RELIABILITY, PB-FREE, HALOGEN-FREE SOLDER** *continues*

could be seen between SAC and SnPb alloys. Analysis of the data showed that, depending on the test vehicle configuration and the test conditions in some cases, SAC alloys gave improved reliability over SnPb alloys and in other examples the reverse result occurred. This testing focussed on environmental conditions representative of the bulk of the electronics industry at that moment in time (-40°C to +125°C). More recent developments in electronics, especially within the automotive sector have pushed these requirements to increasingly harsher test conditions, with 150°C maximum temperature becoming the norm and the number of thermal cycles increasing from 2000–3000<sup>[4]</sup>. In addition, to the increasing environmental conditions, the number of printed circuit boards (PCBs) per vehicle and complexity thereof has increased significantly over the past 10 years as demonstrated in Figure 1. This increased thermal cycle resistance requirement in conjunction with

the expansion of the life-critical nature of the electronics systems within a standard vehicle (ABS, ESP, airbag sensors, lane departure, crash prediction, etc.) has driven the development of improved lead-free alloys for high-reliability applications. In addition to this, reductions in available space and requirements for increased functionality have driven PCB designers to look at component miniaturisation and finer-pitch devices. This is the same trend that was observed in the telecommunications sector over the past 15–20 years. The effect of placing components closer together in harsh environmental conditions has increased the focus on developing fluxing systems with better electrical reliability. The combination of alloy developments that increase the PCBs time to mechanical failure and flux technology that reduces electrochemical failure mechanisms has provided a synergistic system ideally suited for the demands of modern, high-reliability electronics.

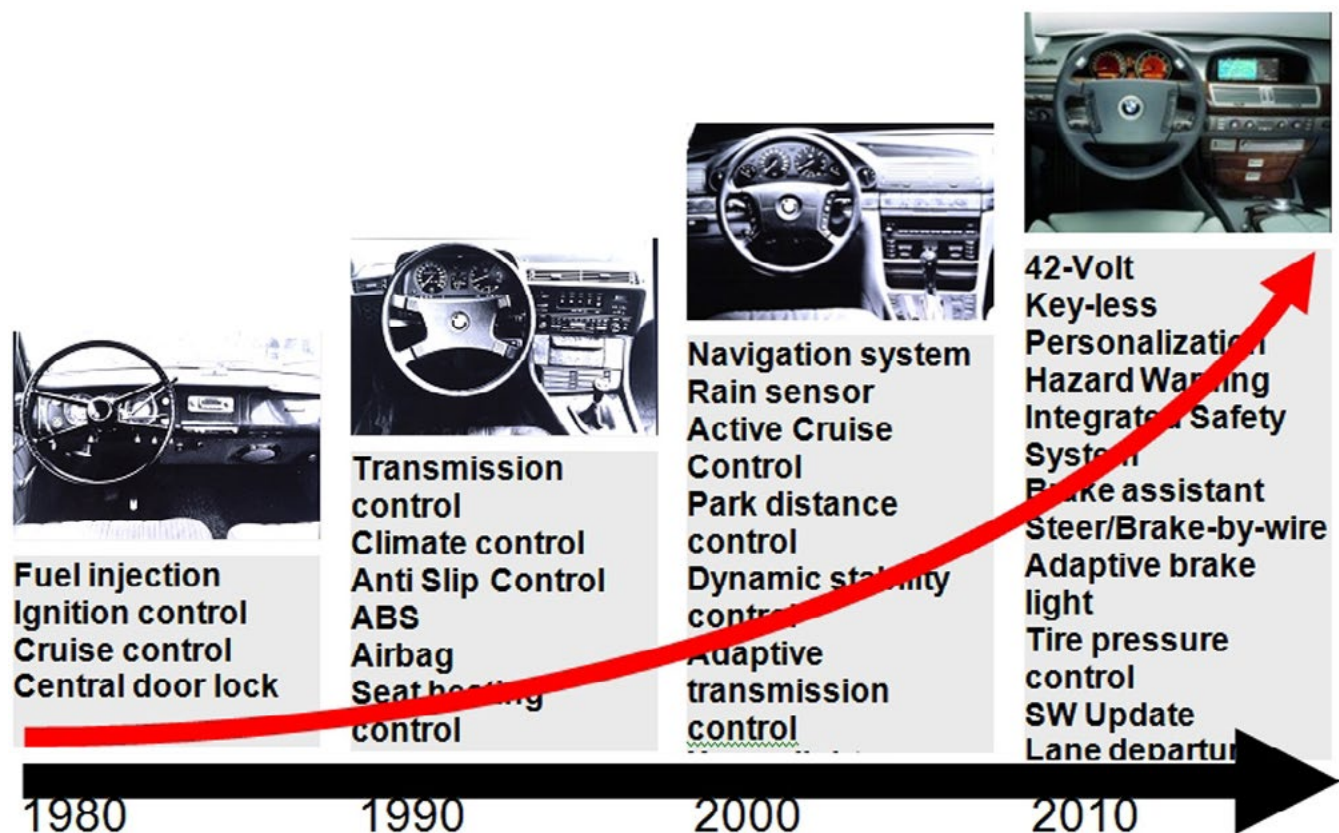


Figure 1: General trends in automotive electronics.

Pictures courtesy of BMW AG



### Alloy Development

The new high-reliability alloy was developed in conjunction with a consortium of partners including academic institutions, end-users and solder manufacturers. The constraints on the project focused on ensuring that the melting point of the new material was equivalent to standard SAC alloys and was capable of operating at temperatures up to 150°C. Furthermore, the alloy also had to be RoHS compliant and contain no toxic or cost-prohibitive elements.

The proposed method of developing the alloy was to focus on the relationship between plastic strain under thermal cycling and number of cycles to failure as defined by the Coffin/Manson equation<sup>[5]</sup>; as shown in Figure 2. The plastic strain imparted into the solder joint is inversely proportional to creep resistance. Therefore, increasing creep resistance will increase the number of cycles to thermal failure. The target for the new alloy development was to match the plastic strain at 120°C peak cycle temperature for standard SAC with a new alloy at peak operating temperature of 150°C. Creep resistance improvement in alloys can be achieved using a number of well-established methods, such as solid solution strengthening, precipitation of doped elements for further alloy hardening or grain refinement. The third option (grain refinement), was discounted be-

$$(N^f)^c \Delta \varepsilon^{pl} = \text{constant}$$

$$(N^f)^c = \text{Number cycles to failure}$$

$$\Delta \varepsilon^{pl} = \text{Plastic strain per cycle}$$

Figure 2: Coffin/Manson equation for crack growth in terms of plastic strain.

cause this option is not applicable to high temperature applications as the grain structure becomes more dynamic with increasing temperature.

The chemistry of Sn-based solder alloys is well-established, limiting the number of co-alloying elements available. After rejection of a number of candidate materials predominantly due to cost, toxicity and excessive melting point adjustment, three candidates of Bi, Sb and Ni were selected.

### Alloy Optimization

Both Bi and Sb showed improved creep resistance, due to solution hardening of the tin-based alloy as shown in Figure 3. The addition of Ni to the alloy does not initially appear to

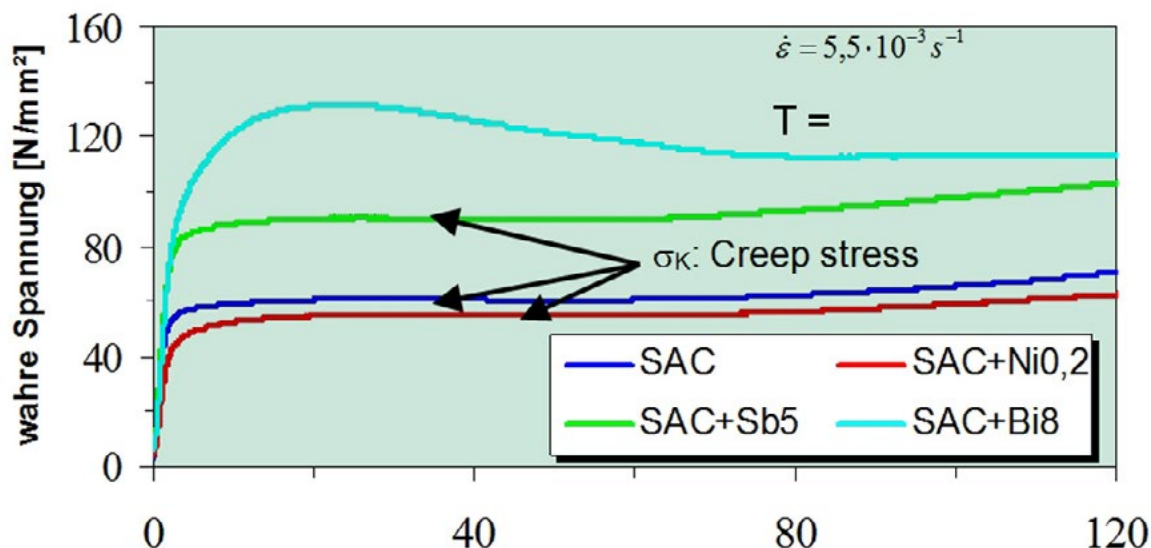


Figure 3: Compressive creep analysis of doped SAC387 alloys.



Confirmation of the physical properties of the novel senary element alloy as a direct comparison to standard SAC387 and SnPb alloys is shown in Figure 5. The creep resistance of the new high-reliability alloy at  $\sim 150^{\circ}\text{C}$  is equivalent to that of SnPb at  $80^{\circ}\text{C}$  as defined by  $s_k$  (creep stress as a function of temperature).

Extensive testing of the alloy for reliability using a range of test vehicles and conditions de-

Flux formulations underpin the entire performance of the solder material, the organic



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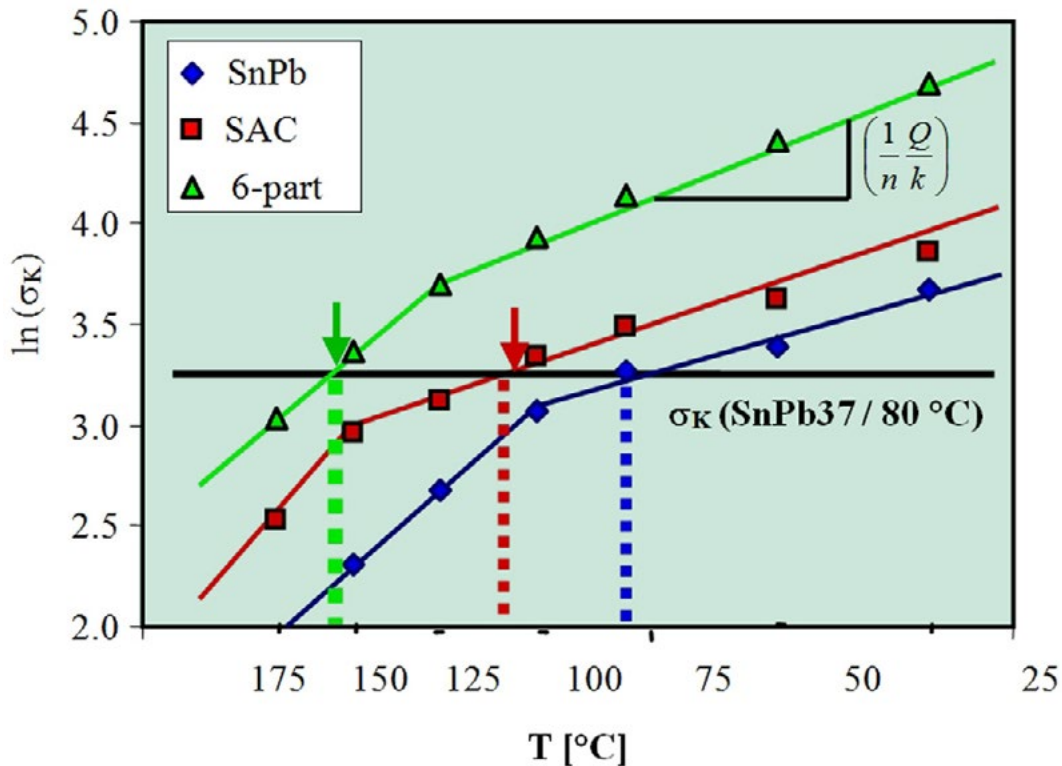
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Figure 5: Creep resistance as a function of temperature.

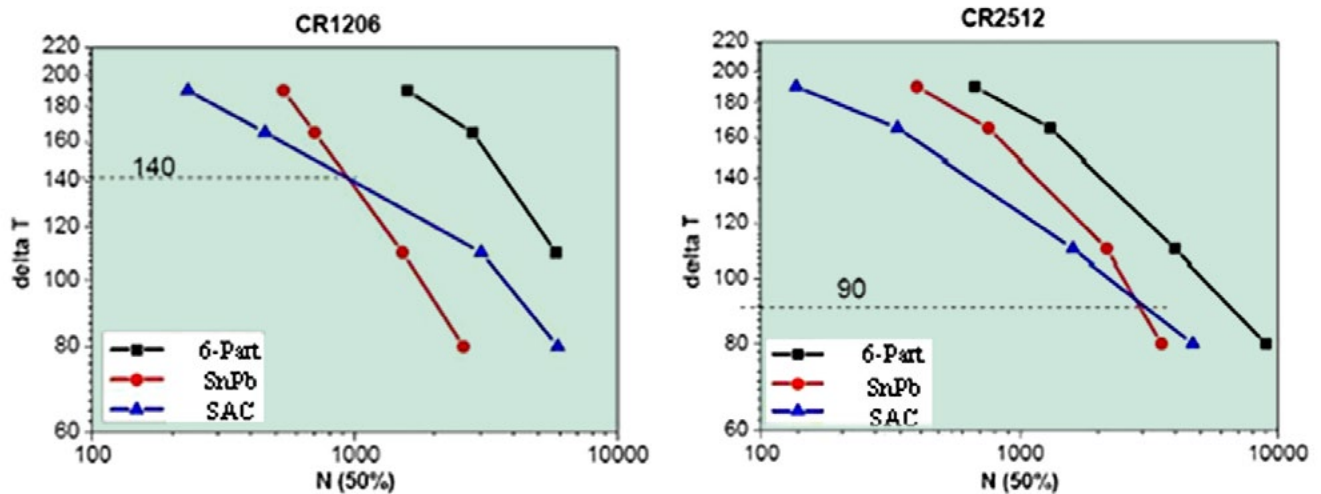


Figure 6a and b: Comparative failure rates for SnPb, SAC and high-reliability six-part alloy in 1206 (a) and 2512 (b) type components assembled on OSP PCBs.

part of the solder paste which only comprises of approximately 12% of the formulation (w/w) determines the printing characteristics, reflow performance and the critical electrochemical

reliability of the final assembly. The successful formulation strategy of a solder paste relies on the material being 'active' towards a range of metal oxides typically found on PCBs and elec-



tronic assembly components. Simplistically, these materials reduce metal oxides to elemental metal to allow the soldering process—namely solder wetting and complete joint coalescence—to occur. The most common oxide-active chemical groups used in the soldering process are carboxylic acids and halogen-containing molecules. Carboxylic acids de-protonate to form the carboxylate ion and a free proton; during the soldering process a metal carboxylate complex is formed with water as a bi-product. Typically organo-metallic salts are readily soluble in the resinous flux matrix and are inherently safe from the point of view of post-soldering electrical and electrochemical reliability. A similar reaction occurs when considering halogen-based active materials; ionic halides also form metal salts and are ‘neutralised’ by the resinous system post-soldering.

There are two main drivers focussing on the elimination of halogen from soldering products. The first is environmental due to the potential for residual halogen- producing poly-halogenated dioxins during PCB incineration. This driver is predominantly focused on polybrominated flame retardants but does impact solder flux formulations. The second is performance. Some early indications show that trace halogens (and potentially halides) can contribute to increased potential for electrochemical migration and corrosion potential as PCBs transition to finer pitches and higher voltages.

### Flux Development Changes

When halogen is removed from a flux, it cannot simply be replaced with other metal oxide active molecules. The halogen-containing compounds are very stable within the flux prior to reflow because the halogen is covalently bonded. Therefore, simply replacing the halo-

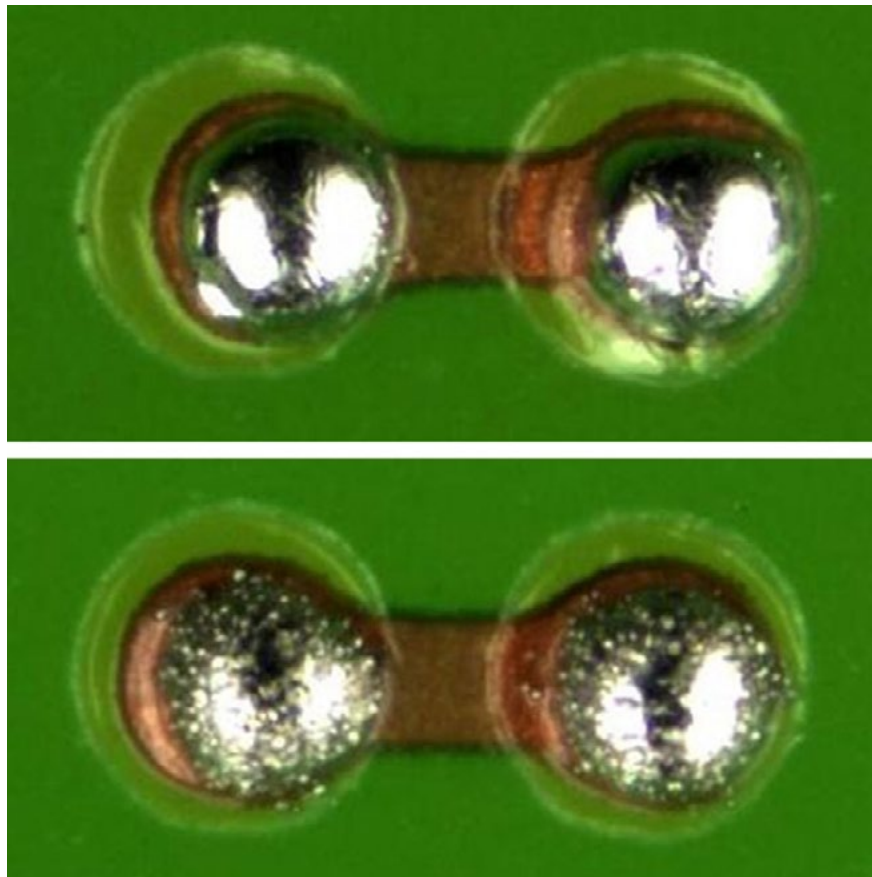


Figure 7: Comparative reflow of halogen-containing solder paste (top) and an equivalent halogen-free (bottom) solder paste.

gen-containing compounds with other activator types can often reduce stability and thus present challenges rebalancing the formulation. Moreover, halogens are exceptionally efficient at oxide removal and offer significant reflow performance benefits. Figure 7 presents an example of the reflow performance of a standard no-clean, halogen-containing reflowed solder joint in a typical aerobic profile as a direct comparison to the identical formulation with the halogens removed. The PCB used for this testing was a standard FR-4 PCB with OSP copper solderable pads. The profile used is a typical aerobic linear profile for SAC alloys. Figure 8 presents the relative wetting speeds of the two pastes using an industry standard wetting balance tester onto oxidised copper substrates. It is evident that the halogen-containing material shows complete coalescence of the alloy and acceptable wetting onto the substrate. In

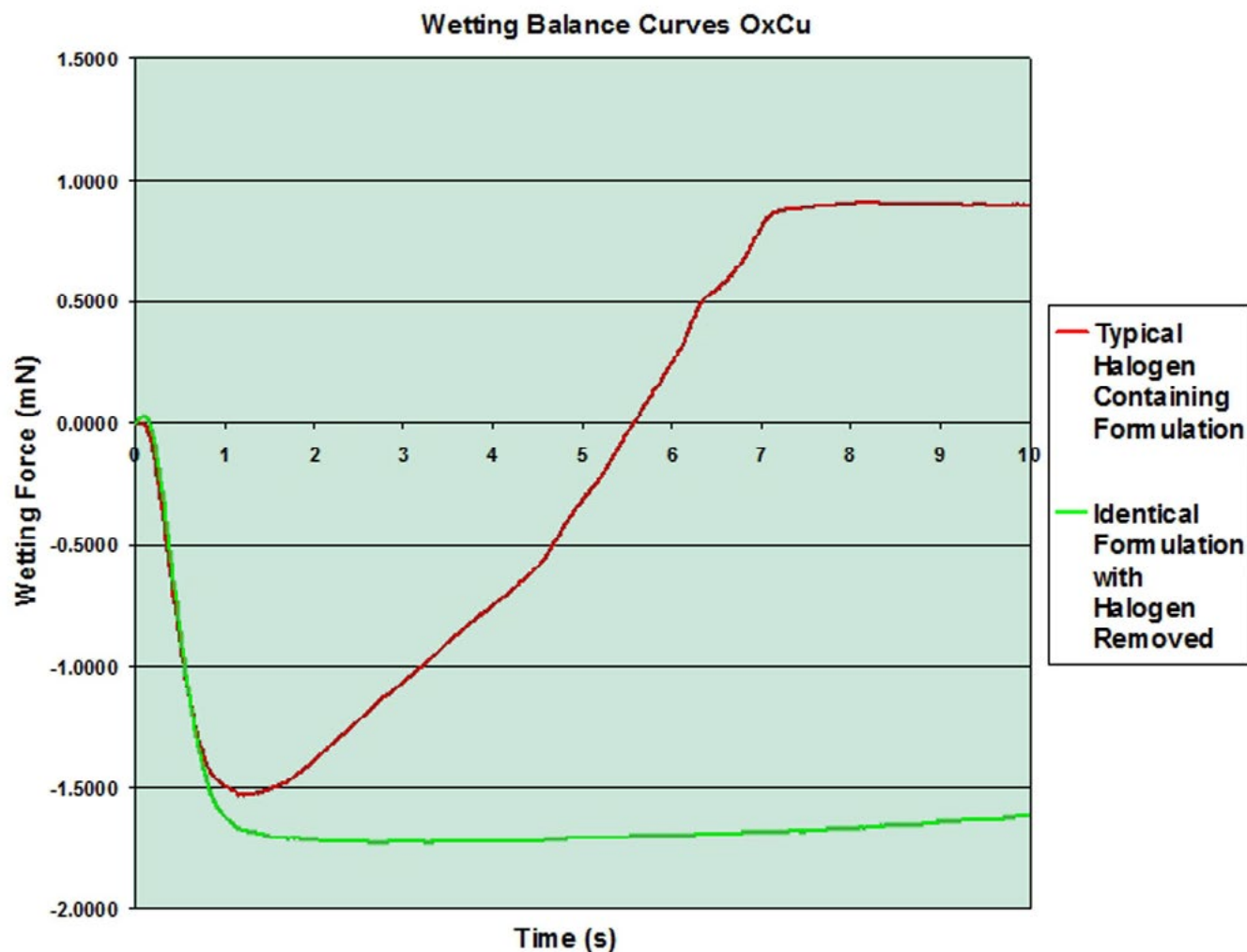
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Figure 8: Comparative wetting balance curves of halogen-containing and non-halogen flux systems.

comparison, the equivalent halogen-free material shows poor coalescence, reduced wetting (spread) and evidence of off-pad solder balling. The wetting speeds of the two materials are also vastly different. The halogen-containing material exhibited fast wetting with a positive wetting force being observed and the halogen-free material showed no positive wetting (and therefore no evidence of oxide removal).

Taking these two performance effects into consideration, the simple approach would be to compensate for the lack of halogen by increasing the remaining proportion of metal oxide active constituents. In principal, this approach to formulation strategy would actually achieve the desired goal of returning the reflow performance

of a halogen-free solder material back to the levels of traditional halogen-containing products. In practice the solution is not this simple. The level of active materials that can be added to a solder paste is governed by two main contributing factors: (1) ensuring the material is electrically reliable as previously mentioned in this paper and (2) guaranteeing the product remains stable for the duration of the storage life. Flux systems are designed to not only remove the oxides from the solderable surfaces of the components and PCBs, but also from the surface of the solder particles within the paste. During reflow, this ensures that the solder alloy will coalesce into a single solder joint. This reaction occurs at room temperature, albeit significantly slower



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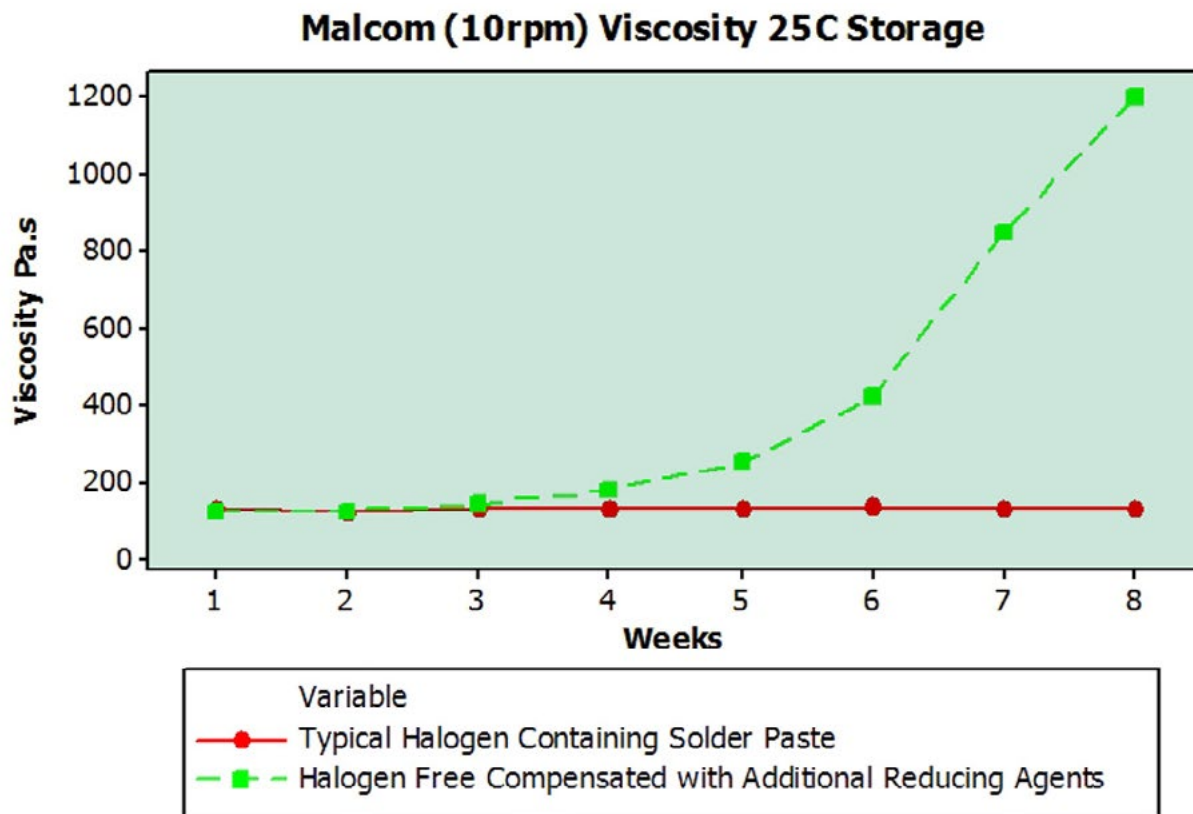
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Figure 9: Comparative stability of standard products versus high activity (non-stable) test material.

than during the reflow process, and is further retarded by storage of the product at temperatures below ambient. As the reaction between the fluxing system and the powder progresses, a matrix-type structure is formed between the active ingredients and the solder powder. This results in a gradual increase in viscosity over time, ultimately leading to a material that would be unsuitable for use in either the print or dispense application in the production environment. Figure 9 details the comparative storage stability of a standard solder material and an equivalent halogen-free system where the level of activity has been increased to compensate. It is clear that the process suitability of the doped halogen-free system has been compromised: the viscosity of the system is seen to increase exponentially over a relatively short period of time.

### Current State-of-the-Art

Significant resource has been dedicated to developing a new generation of solder materi-

als that are completely free of any intentionally added halogen (none detectable under O<sub>2</sub> bomb analysis). Halogen-free materials are permitted to contain up to 900ppm Br, F and 1500ppm (Cl+Br). The approach of formulating with zero intended halogen is undertaken to prevent any localised regions of halogen or halide being present in the reflowed residue. The zero halogen formulations have also been designed to exhibit excellent reflow performance without detrimentally affecting the inherent stability of the products. In addition, these materials have also been developed to be compatible with the new Pb-free high-reliability alloy as documented within this paper. Figure 10 gives representative examples of the soldering performance of the new halogen-free materials using both standard SAC and high-reliability (90iSC) alloys, reflowed using the same process conditions used for the previous examples of reflow. It is apparent that the reflow quality of the new materials utilising SAC-based alloys is comparable—if not



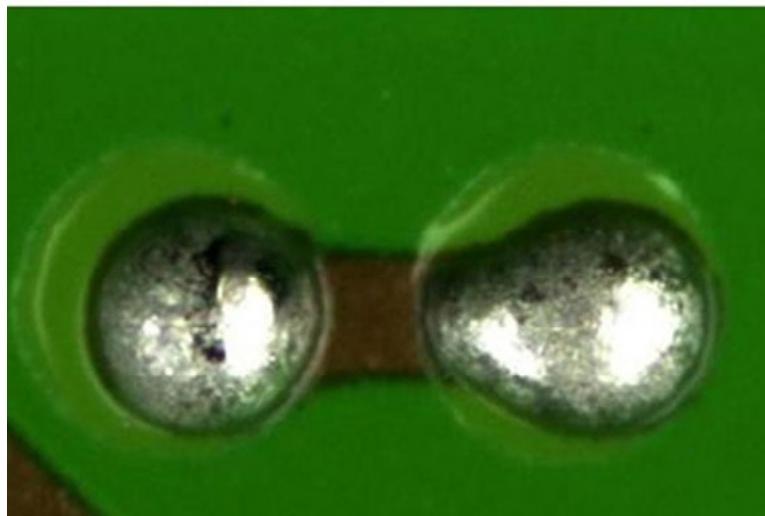
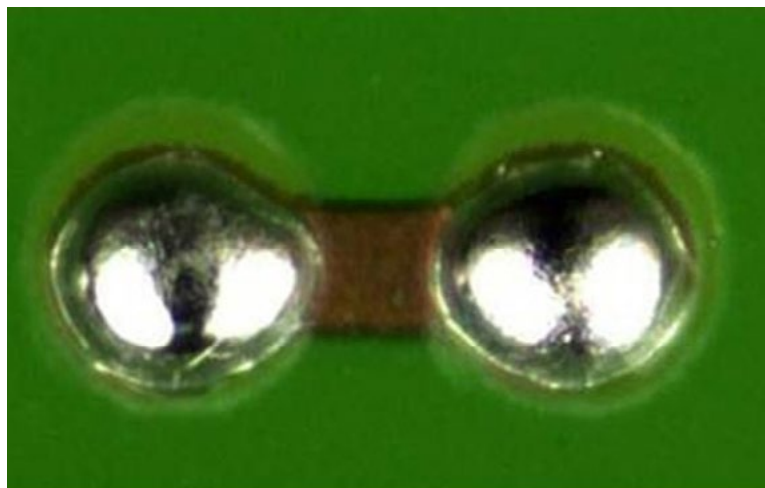


Figure 10: Comparative reflow of halogen-free solder pastes utilising standard SAC (top) and high-reliability 90iSC (bottom) alloys.

superior—to the older generation of halogen-containing solder materials. In addition, the reflow performance of the halogen-free materials with the high-reliability alloy is also particularly good. It should be noted, however, that the high-reliability alloy solder joints look less shiny than standard SAC joints because of the slightly non-eutectic nature of the alloy. This is a factor of the alloy and not the fluxing system.

## Conclusions

Increasing utilisation of electronics in high-reliability applications—especially within the automotive sector—has driven the development of higher-reliability solder products. The

combination of the novel (90iSC) alloy pushes the boundary of thermal cycle and thermal shock resistance. The utilisation of the new halogen-free flux platforms offer reduced risk of electrochemical failures associated with trace levels of halide species present in the post-reflow flux residues. The combination of the new 90iSC high-reliability alloy in combination with cutting edge halogen-free flux platforms signify the future trends for harsh environment/safety-critical electronics. **SMT**

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## News Highlights



### **Orbit to Delist From Nasdaq, Deregister From SEC**

Orbit International Corporation intends to voluntarily delist its common shares from the Nasdaq Capital Market and to subsequently deregister its common stock under the Securities Exchange Act of 1934, as amended.

### **Crane Aerospace Invests in ACE Selective Soldering System**

The new KISS-102 selective soldering system has been installed at the Crane Aerospace & Electronics manufacturing facility in Lynnwood, Washington, and is the second selective soldering machine Crane Aerospace has ordered from ACE Production Technologies.

### **Sparton, Ultra Electronics JV Wins \$26.2M Contract**

Sparton Corporation and Ultra Electronics USSI, a subsidiary of Ultra Electronics Holdings plc (ULE), announce the award of subcontracts valued at \$26.2 million from their ERAPSCO/SonobuoyTech Systems joint venture.

### **Pasternack Earns Excellence Award from Raytheon**

Pasternack Enterprises, Inc. has been awarded the 4-Star Supplier Excellence Award by Raytheon's Integrated Defense Systems (IDS) business.

### **Douglas Electrical Components Earns IPC 620 Certification**

The IPC-A-620 program is the only industry quality assurance standard for cable and wire harness fabrication and installation agreed upon by members of the IPC and the Wire Harness Manufacturers' Association.

### **QCG Achieves AS9100 Rev C Certification**

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### **AIT Presents Conformal Coatings for Extreme Environments**

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### **Ducommun Recognized for 9S-7 RAIDER Helicopter Role**

Ducommun Incorporated was recognized by Sikorsky Aircraft, a subsidiary of United Technologies Corporation, for its role as a critical partner on the S-97 RAIDER helicopter program.

### **Kitron Secures New Order for Kongsberg Gruppen**

Kitron has received a new order worth approximately NOK 51 million from Kongsberg Gruppen for delivery of electronic modules that are part of Kongsberg's weapon control system Remote Weapon Station (RWS).

### **DARPA Unveils Tool to Identify Counterfeit Electronics**

"The Advanced Scanning Optical Microscope—one of many IRIS--developed technologies--offers important hardware security and reliability assurance capabilities," said Kerry Bernstein, DARPA program manager. "These tools are optimized to support the mission of ensuring trust in microelectronics in DoD labs such as NSWC Crane."





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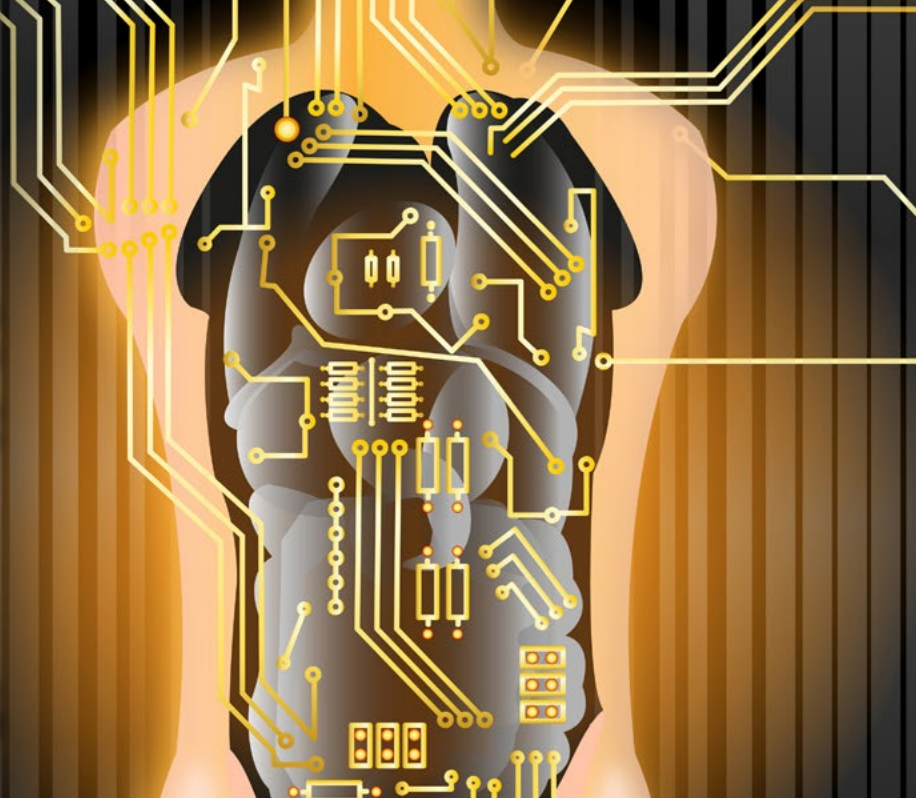
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# Advances in Acoustic Imaging of Medical Electronics



**by Tom Adams**  
SONOSCAN INC.

When a medical electronics system fails in service, the cause of failure is often a broken connection within a plastic-encapsulated component package, and the breaking of the connection is often caused by a structural defect in the package material. Typically, a structural anomaly in the plastic package itself has grown or changed until it caused the connection break. What the user of the electronics system observes is a monitoring device that begins to give erratic readings, a blood pressure sensor that fails, or an implanted electronic device that stops working.

For this reason the individual components are often screened before surface-mounting to remove the ones with internal structural anomalies. The anomalies include delaminations, voids, non-bonds, cracks and other gap-type features. The screening is typically done by an acoustic micro imaging tool such as those in Sonoscan's C-SAM® series.

The key to acoustic imaging is that an interface between two different materials will reflect a predictable portion of an ultrasonic pulse beamed into the component package. The percentage of the pulses reflected is determined by the density and acoustic velocity of the two

materials. At an interface where the protective plastic mold compound is well bonded to the die face about 48% of the pulse to about 70% will be reflected in amplitude mode imaging, the most frequently used mode. The remainder of the pulse will go deeper and be reflected by the next interface. The reflections—the return echoes—are used to give a pixel color value to each of the thousands or millions of x-y coordinates that are scanned by the system's ultrasonic transducer.

Well-bonded interfaces between two solid materials are typically some shade of gray. A technician looking for a questionable component will look for areas of bright white, the signature of gap-type defects that occur when the interface is between a solid and air or another gas. The properties of, say, mold compound and air are so different that essentially all (>99.99%) of the ultrasound is reflected. The imaging process is nondestructive, and the technician viewing the acoustic images can remove the components that meet his company's definition for rejection. Alternately, especially when the lot size is large, the "viewing" and decision-making can be performed by software analyzing the acoustic imaging data.

The components that can be imaged acoustically include IC packages (plastic, ceramic and polyimide), ceramic chip capacitors, some types of resistors, and most recently IGBT mod-





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## ADVANCES IN ACOUSTIC IMAGING OF MEDICAL ELECTRONICS *continues*

ules for high-power applications. Before surface mounting, the components are screened on a laboratory acoustic system if the numbers are small or by a semi-automated or fully automated system if the numbers are large. The idea is to remove from assembly those component packages whose delaminations, voids or other anomalies are likely to cause eventual electrical failure. Electrical testing can't find these structural defects unless they have already caused a failure. An engineer examining acoustic images will routinely see component packages having single defects (a die face delamination, for example) or having multiple defects (many delaminations along the lead finger and on the die paddle). But if no electrical connection has yet been broken, all of the defective components would pass electrical testing.

Below are details of three areas in which new acoustic techniques or technologies are being used to image and analyze advanced components.

MEMS (microelectromechanical systems) are sensors built with semiconductor technology. In many applications, they replace much larger systems and do so with significant cost savings. An early and still important MEMS application was the accelerometer used to activate air bags in cars. MEMS devices are widely used in medicine to measure blood pressure inside a patient's intravenous line. Among the numerous other medical applications are measurement of fluid pressure during eye surgery, measuring a baby's blood pressure during birth, and monitoring a respiration when a ventilator is in use.

A MEMS device typically has a cavity that contains a mechanical element, usually in a vacuum, and that is connected to electronics that pick up the signal from the device. The cavity is etched into a silicon die. During assembly of the MEMS device, a seal is typically placed around the cavity to preserve the vacuum (or in some cases a gas) that is necessary for its functioning. A cover plate, which may be silicon or glass, is then placed on top of the die, thus forming the seal. During acoustic imaging, the cavity behaves as a large gap, and the interface between the gap and the silicon above it will be bright white.

The contents of the cavity are not usually of interest acoustically, but the condition of the

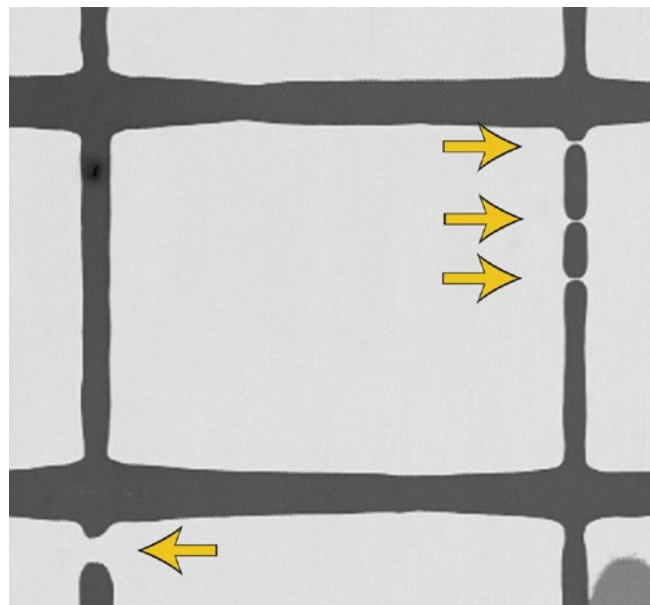


Figure 1: An acoustic image encompassing the seals around several MEMS devices. The sample was a MEMS wafer before dicing. The arrows point out gaps in the seals.

seal around the cavity is. The long-term reliability of the MEMS device depends largely on the integrity of this seal. As MEMS dimensions have shrunk, acoustic imaging has adapted to image seals that may be as narrow as six microns.

The seal material needs to be well bonded to both the cavity die and the cover plate. It also needs to be free from any voids or other gap-type defects that could cause it to leak at some time in the future. An acoustic micro imaging tool is used to look for these defects. Ultrasound pulsed into one side of the device is gated on the full thickness of the seal, including the interfaces at the top and bottom of the seal of the seal, and the bulk material of the seal. These interfaces should be displayed as some shade of gray in the acoustic image. But any voids or other gaps in the seal itself will appear as bright white areas—a circular void, for example. In some instances, the defect takes the form of missing material.

Insulated gate bipolar transistors (IGBT) are high-power semiconductor switches used in MRI systems and other high-power applications. The switching element can be a silicon (Si), silicon carbide (SiC) or gallium nitride





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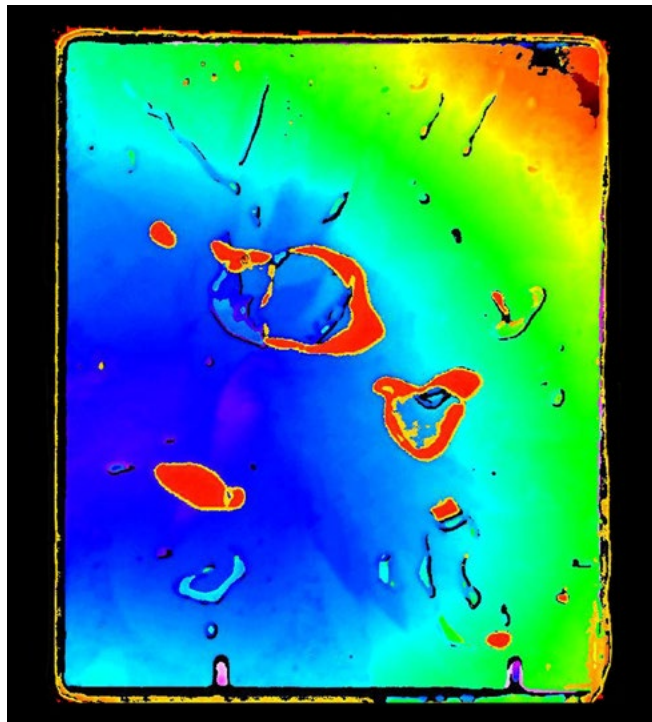
ADVANCES IN ACOUSTIC IMAGING OF MEDICAL ELECTRONICS *continues*

Figure 2: Acoustic image of the solder layer between the heat sink and the raft in an IGBT module. Irregularly shaped features are voids in the solder; colors indicate distance to the raft, and thus the thickness of the solder.

(GaN) die that, because of the high power, must dissipate a great deal of heat.

There are many types of high-power IGBT modules, but they generally have a three-layer structure, with the die resting on a ceramic raft, which in turn rests on a metal heat sink. Additional layers of material include the adhesive bonding the die to the raft, and the solder or other adhesive bonding the raft to the heat sink. These assemblies are imaged acoustically before encapsulation in a plastic package that will cover everything except the heat sink.

The heat generated by the die must flow downward, through the raft and the heat sink. Much less powerful assemblies can fail if they overheat; the bonding of the elements in the module must be very good. The typical defects are voids or other gaps in the adhesive materials, or the tilting of the ceramic raft. Finding gap-type defects here before encapsulation of the module is critical because the module can still be reworked.

Until recently, though, high-power IGBT modules generally could not be imaged by acoustic micro imaging tools. The problem was the die's sensitivity to contamination. The transducer of an acoustic system must be coupled during scanning to the surface of the part by a small column of water. But the power used in IGBT modules is so high that even the faintest residue left by the momentary passage of a water column could later become a leakage path. (Note that there are also lower-power IGBT modules, used for example in audio and automotive applications, where these restrictions do not apply.)

To make high-power IGBT modules inspectable, Sonoscan designed an acoustic micro imaging tool whose transducer points upward and is accompanied by a small water jet to create an upward-flowing column to couple the transducer's ultrasound to the metal heat sink at the bottom of the IGBT module. The module (or modules; the system can have two transducers) rests in a cutout in a plate above the transducer. There is no path by which water can reach the module's die, and ultrasound pulsed into the heat sink can image features up to and including the die attach.

Figure 2 is the acoustic image showing the solder layer between the heat sink and one ceramic raft on a high-power IGBT module. The solder (or adhesive) layer is of great interest because defects here can block the dissipation of heat from the die.

The irregularly shaped features of various colors are voids (air bubbles) in the solder. They vary in color because Sonoscan's Time Difference software is being used to display the distance of a feature from the transducer, instead of the amplitude of the signal. The red voids are nearest to the transducer (i.e., near or in contact with the heat sink). Other voids are deeper within the solder. But the color also measures the depth of the raft's surface, and thus the thickness of the solder. The solder is thickest in the dark blue regions at left, and thin or lacking at the upper right. Conclusion: the raft is tilted, and voids are present—both conditions that will impair heat dissipation.

Integral mode imaging offers advantages in situations where it is desirable to more ac-



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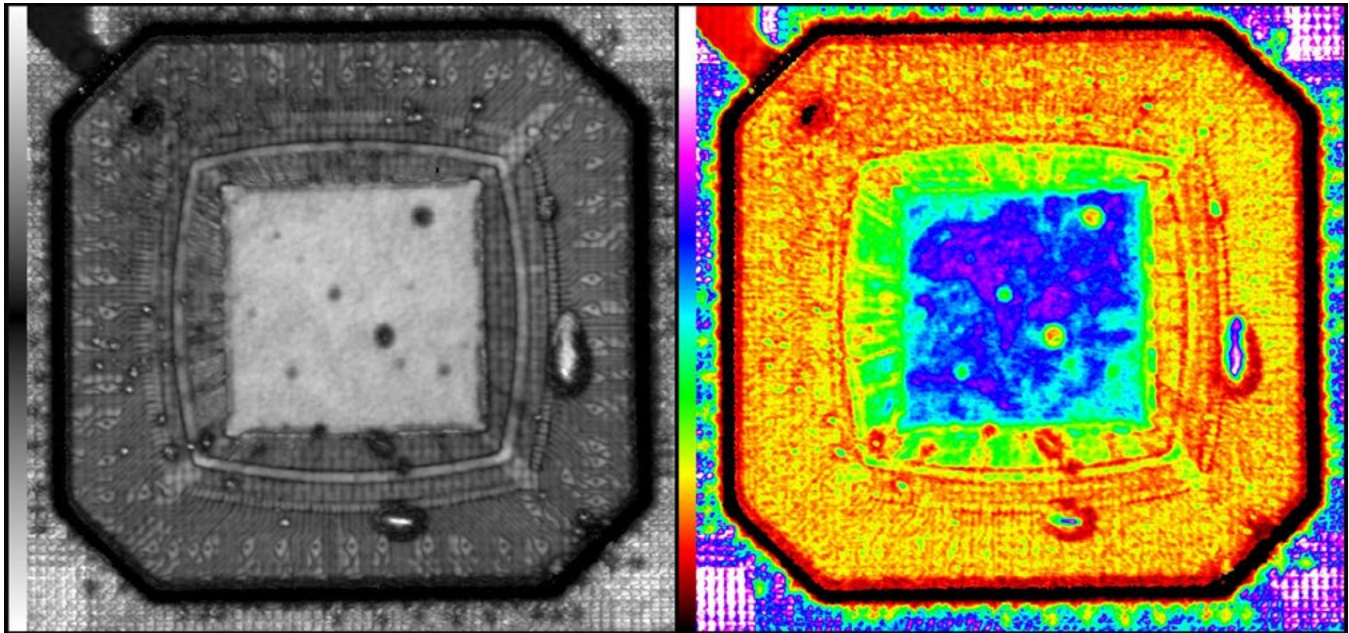


Figure 3: Standard amplitude mode imaging shows the square die region as bright gray (left), but integral mode imaging reveals the dark blue delamination below the die (right).

curately see and analyze anomalies in components. Suppose there is a delamination at the substrate level in a plastic BGA package. Standard amplitude mode imaging will scan the component and assign a pixel value, based on signal amplitude, to each of the x-y coordinates into which it pulses ultrasound. The pixel value will correspond to the single highest amplitude found among the many echoes received from each x-y coordinate at the level of the delamination. This is standard imaging practice and in most situations gives excellent results. But some components, and particularly those going into critical roles such as medical applications, will respond better to an improved and more subtle approach using the integral mode.

Integral mode uses the sum (rather than the average) of the amplitude of all the echoes received from the depth of interest to assign the pixel value. A delamination imaged first in standard amplitude mode may show the same bright white delamination, but integral mode may show a zone of irregularities—varying shades of gray, for example.

Figure 3 shows, at left, the standard amplitude mode image of a plastic BGA package, gated to include depths from mold compound-die

interface to the die attach-substrate interface. Within the square area of the die at center are seen the dark acoustic shadows of a few voids in the mold compound above the die, along with the rather bright image of the mold compound-die interface. Because of the physical properties of these two materials, most of the ultrasound is reflected, and only perhaps 25% travels deeper. There are some slight irregularities in the gray areas here, but they are too faint to interpret.

At right in Figure 3 is the integral mode image of the same depth. By using the sum of the echoes received at each pulse location, this method shows a dark region that indicates a delamination somewhere below the die face. By making an A-scan (i.e., single pulse) waveform of a few locations within the apparent delamination, it was possible to tentatively identify the delamination as lying within the die attach rather than within the substrate below. **SMT**



Tom Adams is a consultant for Sonoscan.



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# TOP TEN

## News Highlights from SMTonline this Month

### ① **IPC Honors Significant Contributions by Volunteers**

IPC presented Committee Leadership, Special Recognition, and Distinguished Committee Service Awards at the association's Fall Standards Development Committee Meetings in Rosemont, Illinois. The awards were presented to individuals who made significant contributions to IPC and the industry by lending their time and expertise in the development of standards.

### ② **Soneter Enters Strategic Partnership with Flextronics**

"We are eager to be entering the next phase of our company's growth and are excited to be able to meet the needs of our customers," said Jeff Leaders, president and CEO. "The partnership with the GRA Venture Fund and the strategic partnership with Flextronics will enable us to rapidly advance our offerings."

### ③ **NATEL EMS Implements Kaizen Philosophy**

NATEL EMS empowers employees to improve processes that in turn improve reliability. By giving everyone involved the ability to improve a process, the accumulated sum of these small changes makes a huge impact on both the quality and reliability of the end product.

### ④ **U.S. House of Representatives Passes RAMI Act**

The U.S. House of Representatives passed H.R. 2996 the Revitalize American Manufacturing and Innovation (RAMI) Act. Viewed as a critical piece of legislation in America's renewed effort to preserve and recapture manufacturing jobs, the RAMI Act focuses efforts to spur innovation and capitalize on emerging manufacturing technologies.



## 5 Congress Meets on NNMI; Highlights Activities of IMIs

The industry and institute panelists addressed the benefits and impacts of the NNMI, highlighted the activities of the four recently established IMIs, and expressed the need for the pending RAMI Act to be enacted into law.

## 6 Flextronics, Mantis Vision Collaborate on 3D-enabled Tablet

Mantis Vision and Flextronics have announced their collaboration and development of the revolutionary, OEM-ready, 3D-enabled tablet specifically designed for Dynamic 3D Content Creation, called Aquila.

## 7 PartnerTech Achieves ISO 13485 Certification

By achieving ISO 13485, PartnerTech Inc. proved the highest level of requirements in a quality management system designed specifically for the manufacture of medical devices and related services to consistently meet customer and regulatory requirements.

## 8 AlphaEMS Achieves ISO-13485 Certification

This internationally-recognized certification was awarded to the company upon demonstration of its ability to deliver PCB assembly services that consistently meet customer specifications and regulatory requirements applicable to medical devices and related industries.

## 9 Sanmina Wins Award for Supplier Quality from EchoStar

EchoStar, a premier global provider of satellite operations and video delivery solutions, honored Sanmina with its Gold Award, given in recognition of the company's high performance in product quality and manufacturing excellence for products produced in its Kunshan, China facility.

## 10 EMS Industry Reports Sluggish Growth of 4.9% in 2013

The worldwide EMS market is a determining force in production of electronics products and now accounts for almost 40% of all assembly. The industry expanded approximately 4.9% in 2013 as a result of a downturn year when normal growth could easily have been double without decline in demand for computer desktop and notebook products.

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# EVENTS

For the IPC's Calendar of Events, click [here](#).

For the SMTA Calendar of Events, click [here](#).

For the iNEMI Calendar, click [here](#).

For a complete listing, check out *SMT Magazine's* full events calendar [here](#).

## **LaserJob Technology Forum**

November 6, 2014  
Furstenfeld, Germany

## **LA/Orange County Expo & Tech Forum**

November 6, 2014  
Long Beach, California, USA

## **36th International Electronics Manufacturing Technology Conference**

November 11–13, 2014  
Johor, Malaysia

## **International Wafer-Level Packaging Conference**

November 11–13, 2014  
San Jose, California, USA

## **TSensors Summit 2014—San Diego**

November 12–13, 2014  
La Jolla, California, USA

## **Wearable Sensors and Electronics 2014**

November 12–13, 2014  
Santa Clara, California, USA

## **ELECTRONICA 2014**

November 11–14, 2014  
Messe Munchen, Germany

## **High-Reliability Cleaning and Conformal Coating Conference**

November 18–20, 2014  
Schaumburg, Illinois, USA

## **Graphene LIVE! 2014**

November 19–20, 2014  
Santa Clara, California, USA

## **International Printed Circuit & APEX South China Fair**

December 3–5, 2014  
Shenzhen, China





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