

# DesignCon 2007

## Comparing Time-Domain and Frequency Domain Techniques for Investigation on Charge Delivery and Power-Bus Noise for High-Speed Printed Circuit Boards

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## Abstract

The performance of power distribution network is critical to high-speed digital circuits in terms of both signal integrity and radiated emission. This paper studies charge delivery of a power distribution network, as well as power bus noise resulting from device switching, in the time domain as well as the frequency domain. Some of the PDN performance analysis is easier to understand when analyzed in the time domain. The effects of capacitor location, capacitor value, power/ground plane pair location within the stackup, board size, as well as dielectric material, are discussed.

## Authors Biographies

**James L. Drewniak** received B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois at Urbana-Champaign in 1985, 1987, and 1991, respectively. He joined the Electrical Engineering Department at the University of Missouri-Rolla in 1991 where he is one of the principle faculty in the Electromagnetic Compatibility Laboratory. His research and teaching interests include electromagnetic compatibility in high speed digital and mixed signal designs, electronic packaging, and electromagnetic compatibility in power electronic based systems.

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# 1. Introduction

In high-speed digital circuit designs, the PDN associated with the PCB plays a vital role in maintaining signal integrity (SI), i.e., necessary fidelity of signal and clock wave shapes, and minimizing electromagnetic noise generation. Yet, the design of the power distribution system presents an increasingly difficult challenge for digital circuits employing active devices. As integrated circuit (IC) technology is scaled downward to yield smaller and faster transistors, the power supply voltage must decrease. As clock rates rise and more functions are integrated into microprocessors and application specific integrated circuits (ASICs), the power consumed must increase, meaning that current levels, i.e., the movement of electrical charge, must also increase [1-2].

One category of design engineer who confronts this design challenge is the signal integrity (SI) engineer, whose goal is to ensure adequate fidelity of the individual signal and clock waveshapes on the PCB [2-4]. Another category of engineer who faces similar design challenges is the electromagnetic interference/compatibility (EMI/EMC) engineer, whose goal is to minimize electrical noise generated by the circuitry to prevent interference with other systems and within the same system [5-8]. While both engineers wrestle with the same physics of the dc PDN on a digital PCB, practitioners of different design disciplines may view the same physical phenomena differently. For instance, the SI engineer may be more familiar with circuit behavior and analysis expressed in the time domain than with the behavior of electromagnetic waves and analysis expressed in the frequency domain. The EMI engineer's experience is likely just the reverse. Therefore these engineers may employ different methodologies and approaches to PCB design. These different design methodologies may sometimes seem contradictory and/or incompatible, but both engineers have similar goals of assuring adequate charge transfer between active devices and the PDN with minimum noise generation. This paper is intended to review the state of knowledge of dc power distribution design, offer practical design advice, and address schools of design that appear to offer conflicting advice.

The PDN for modern medium-to-high-speed digital PCBs is usually formed from one or more pair of conducting planes used as power and ground (power return). The PDN for digital circuitry has evolved over time, as signal and clock speeds have increased, from discrete power supply wires, to discrete traces, to area fills and ground islands on single/two-layer slow-speed boards, to the planar power bus structure used extensively in today's multi-layer high-speed PCBs. The low inductance associated with charge delivery from the plane to circuit element allows for the storage of relatively easy-to-deliver charge available all over the board. Often the term power bus is used to identify an individual plane pair, whereas the term PDN is used for the entire system of supplying power to circuits placed on the PCB. As speeds of active devices have increased, digital data rates have escalated and signal rise and fall times dropped so that the frequency regime of operation on the PCB has risen into the gigahertz (GHz) band. Operation at high frequencies can blur the boundaries between circuit behavior and electromagnetic behavior.

Noise is generated in the power bus when a digital active device (integrated circuit or transistor) switches between its high and low logical states (switching noise) [5], or it can be coupled to the power bus when a high-speed signal transits through the power bus by

signal vias (transition noise) [9,10]. Noise generated in the power bus can be easily propagated throughout the board. Propagated noise can affect the operation of other active devices (signal integrity) as well as radiate from the PCB (EMI). At the printed circuit board (PCB) level, there is no way to eliminate the production of noise by IC devices. However, a good PCB design can ensure that the generated noise be constrained to a level that permits successful circuit operation and the resulting low levels of radiation produced do not violate regulatory requirements. The use of decoupling capacitors are one of the key elements in achieving this goal, along with the board stack up design, power/ground plane pair, usage of losses, power islands, board edge termination, etc.

## 2. The power Delivery Network

There are two primary purposes of the PDN. The first purpose of the PDN is functionality. The PDN is a charge storage and delivery system that supplies charge (current) when an IC switches state and requires additional current. If sufficient current is not provided, the IC may experience a functional failure.

A second purpose of the PDN is to reduce or minimize the noise injected into the power and ground-reference plane pair and thus reduce the potential of noise propagation in the board and EMI emissions from the circuit board. The mechanisms for EMI emissions are several. For instance, the edge of a board may be near the seams of a metal enclosure or near an air vent area, allowing this noise to escape the enclosure. Alternatively, PDN noise may couple onto input/output (I/O) connector pins or onto a grounded cable shield and be directly coupled out of the metal enclosure through any of the cables. There are a variety of coupling mechanisms that are possible once this noise is created. To avoid undesirable consequences from noise on the PDN, the impedance of the PDN should be low over a wide frequency range that includes the spectrum of the critical signals and their harmonics.

### The Decoupling Capacitor

A PDN is comprised of several elements, including the VRM module, bulk capacitors, SMT decoupling capacitors, and power/ground plane pairs (power bus). The effectiveness of each element in delivering sufficient charge with adequate speed is not uniform. A charging hierarchy exists based on the rate of charge delivery (usually impeded by distance and inductance) and charge storage capacity [2].

The VRM (Voltage Regulator Module, i.e., dc/dc converter), the largest source of charge, is able to store and release a lot of charge but it cannot meet demands to rapidly deliver charge due to the large inductance connecting it to the PDN. It cannot keep up with charge demands that vary or oscillate with rapidity greater than a MHz. Hence, it cannot deliver charge in a timely manner when the circuits demanding charge have time constants that are much shorter than one microsecond.

Bulk capacitors constitute the second largest source of charges in this hierarchy and are typically capacitors whose values range between a few hundred microFarads to as high as a few milliFarads. These components are able to supply charge with sufficient

speed to meet the demands by systems characterized by time constants as low as a few hundreds of nanoseconds and even shorter.

Decoupling capacitors, sometimes referred to as “high-frequency ceramic capacitors”, are the second to last category of components in this charging hierarchy [2]. Decoupling capacitors usually exhibit capacitance values from a few tens of nanoFarads to as high as a few microfarads. These capacitors can usually support charge demand from circuits with time constants as low as a few tens of nanoseconds.

The PWR/GND planes form the last component in the charging hierarchy and can usually deliver charge to circuits whose time constants are shorter than a few tens of nanoseconds, i.e., a charge demand frequency above several hundreds of MHz.

The VRM and the bulk capacitors are usually few in number and are located in specific areas of the PDN due to their dimensions and other constraints. High-frequency decoupling capacitors are usually large in number and are typically easily located with a greater flexibility. Fig. 1 shows a typical impedance profile of a decoupled PDN.

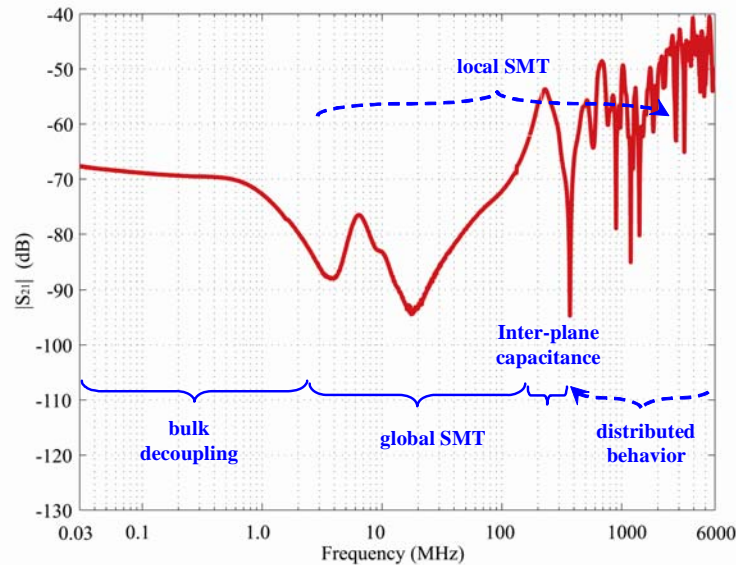


Fig. 1: Typical Impedance Profile for PDN.

Self impedance, or  $Z_{11}$ , provides an indication of the voltage created by the injection of noise current.  $Z_{21}$  indicates the noise transmission from noise source to anywhere on the board.  $Z_{21}$  is very useful for circuit susceptibility and radiated emission studies.  $Z_{ij}$  is a vector quantity in that it has both magnitude and phase. For these types of studies, often just the magnitude is examined. The effect of phase will be discussed later.

The decoupling capacitor exhibits parasitic inductance and resistance in addition to its capacitance. The parasitic inductance consists of an inductance associated with the capacitor itself (equivalent series inductance, or ESL) and inductance associated with the means of connecting the capacitor between power and ground planes (inductances associated with the solder pads used to secure the capacitor to the PCB and any traces and/or vias used to make the electrical connections). The parasitic inductance impedes changes in the current; hence, it impedes the prompt availability of charge. The parasitic

inductance and resistance when combined with the device's capacitance, form a series resonant circuit whose impedance dips to a minimum at the frequency where the inductive and capacitive reactance cancel. Low values in interconnect inductance can often be achieved by careful attention to the design of solder pads lands with low inductance properties along with having no traces in the ideal case, or in the realistic case, very short traces connecting them to the planes [4]. The parasitic inductance of the interconnects can be several nH to less than 1 nH. In brief, a good PDN design is characterized by a low interconnect inductance between each decoupling capacitor and the PDN itself. Fig. 2 illustrates the connection of an SMT capacitor to a power bus which provides a parasitic inductive component from the current path above the plane (Loop 2) and a parasitic inductive component associated with current flow between the planes, first in the via and then returning as displacement current (Loop 1). As stated earlier, the parasitic inductance associated with current flow above the plane also includes effects from the solder pads that connect to the capacitor and any traces used to connect solder pads to the vias. The lower the value of the inductance, the faster the capacitor can supply and store charge and the more importance that is attached to the distance of the decoupling capacitor from an IC in achieving effective decoupling capacitor behavior.

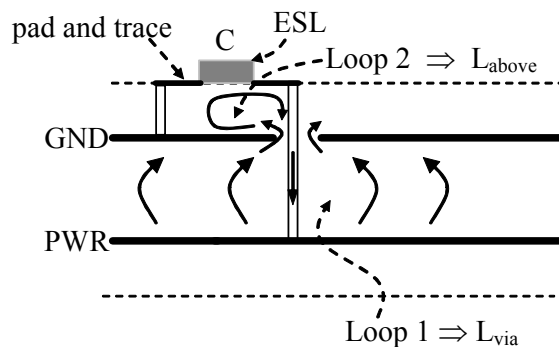


Fig. 2: Connection Inductance Associated with Capacitor Mounting on PCB.

The ESL of the decoupling capacitors is a function of the length, width, height and manufacturing technology of the capacitor itself. Due to improvements in the material selection and manufactory technology, the size of SMT decoupling capacitors have been shrunk from the early 1206 package size (120 mils length x 60 mils width) down to the more recent 0201 (20 mils length x 10 mils width) package size, allowing a significant reduction of the equivalent series inductance, which is always less than 1 nH.

The equivalent series inductance (ESL) as well as the equivalent series resistance (ESR) is usually measured by employing impedance analyzers and/or network analyzers. In both cases, special fixtures are utilized along with calibration procedures and measurement techniques in order to minimize the parasitic elements associated with the measurement setup itself [11]. Values reported by capacitor manufacturers are influenced by the specific measurement techniques employed and should be viewed critically when the use of the specific values of parasitic elements is desired. Typically, the interconnect inductance is significantly larger than the ESL, making the ESL a small portion of the overall inductance.

## Determining Individual Decoupling Capacitor Values – Differing Approaches

### Approach A: The SI community

Two general approaches have developed in the design community on how to deploy decoupling (high-frequency ceramic) capacitors in order to reduce the impedance of the PDN between frequencies in the range of approximately 1 MHz to a few hundred MHz. A prominent approach, referred to here as Approach A, is used in the SI community and has developed out of the experience of server motherboard design and other high performance digital PCBs [2-3]. This approach uses an array of values of decoupling capacitors. This technique generally uses three capacitor values per decade to achieve the flattest PDN impedance vs. frequency profile to maintain an upper bound “target impedance” to provide an upper bound on the AC ripple voltage on the PDN [4, 11].

In Approach A, the capacitor values are typically chosen so that they are logarithmically spaced (i.e. 10, 22, 47, 100 nF, etc). The effectiveness of this approach is somewhat dependant on the value of ESR of the capacitors and the resulting series/parallel resonant (resonant/anti-resonant) frequencies of the decoupling capacitors to maintain the impedance to be below the desired target impedance over the frequency range of interest.

### Approach B: The EMI community

On the other hand, a prominent view in the EMI community for PDN design for high-speed digital PCBs is that the specific values of decoupling capacitors need not be as carefully chosen as in the previous approach [5]. This design methodology, Approach B, addresses the high-frequency ceramic decoupling specifically and employs the largest value of capacitance available in the specific surface mount technology (SMT) package size to yield a PDN impedance profile that is acceptably flat. For the same number of high-frequency ceramic decoupling capacitors, more total capacitance is often achieved in Approach B than with Approach A.

A comparison of the two approaches in the frequency range between 1 KHz and 1 GHz using a 2-D cavity model method, allowing parallel plane characteristics to be included[12, 13]. The PDN dimensions correspond to a PCB that is 6 in. x 9 in. with a single power/ground plane pair power bus of thickness 10 mils. The PCB material is chosen to exhibit a dielectric constant of 4.5, and a loss tangent of 0.02; a relative permeability of unity; and a plane capacitance of 2.426 nF. For each example with this PCB, one bulk decoupling capacitor and 60 ceramic decoupling capacitors were chosen. In addition, it was assumed that the power bus was located at the center of the 62 mil PCB stackup and that all decoupling capacitors were placed on the board’s surface, allowing for inclusion of the via interconnect inductance in the simulation. A target impedance of -20 dB $\square$  was chosen. For each capacitor type, typical values of ESR and ESL were selected from typical values from a specific vendor’s catalog for X7R MLC capacitors. [14]

A third approach, Approach B1, a subset of Approach B, was included to investigate the effects of making all of the smaller decoupling capacitors in the 0402 package size, instead of dividing them between the 0603 (60 x 30 mils) and the 0402 (40 x 20 mils)

package sizes. Fig. 3 shows the driving point impedance,  $|Z_{11}|$  of the PDN. While there are differences between the three approaches shown in the Figure, all three provide an impedance well below the target impedance up to frequencies in the range of 100 MHz. At low frequencies, Approaches B and B1 provide a lower impedance, which is a manifestation of the higher capacitance used. It is also interesting to note that there is very little difference between Approaches B and B1, except near 1 MHz, where the impedance is already very low compared to the target impedance. Above a few MHz, when the impedance rises proportional to frequency, i.e., at a rate of 20 dB/decade, there is virtually no difference between any of the methods. In this example, above 100 MHz, the discrete decoupling capacitors do not do a good job of maintaining a low PDN impedance, regardless of the design strategy.

In these examples, it is clear that either approach can achieve the design goal on PDN transfer impedance and have nearly identical performance above frequencies of a few hundred MHz. Use of a single value of capacitance in the largest value in the package size may provide the benefit of simplicity of design and manufacture [7]. Changing the design parameters (PCB characteristics, power bus characteristics, capacitor characteristics, etc.) will alter the impedance curves regardless of the design approach used, but will not change the overall conclusion that there is little difference in the PDN impedance profiles between Approaches A and B (and B1).

Although the values of the decoupling capacitors employed are different in the two strategies, the need of lowering the parasitic inductance associated with the decoupling capacitors is consistent [2,3,5,8]. In fact, lowering this inductance shifts all the series/parallel resonant frequencies higher and in particular the last one, allowing the PDN to meet the design specifications on the target impedance in a broader frequency band.

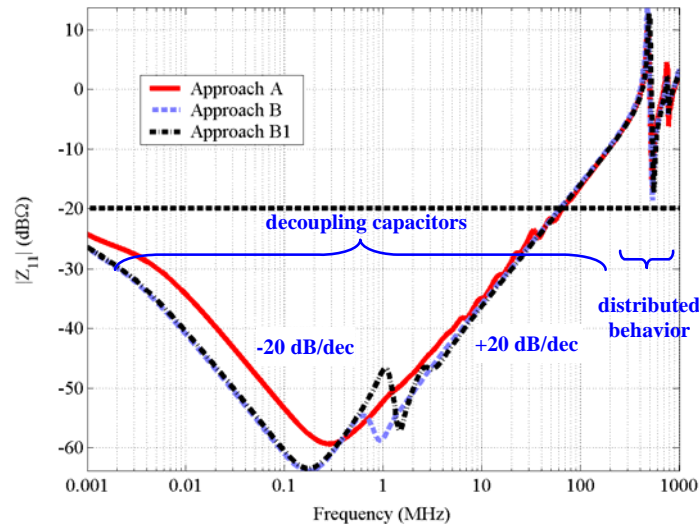


Fig. 3: PDN Impedance from Comparison of Decoupling Approaches.

## The Importance of Capacitor Location

The significance of decoupling capacitor location has been extensively studied in the EMI design community [16, 17]. In the early days of digital electronics on PCBs consisting of only a few layers (and perhaps without power and ground planes), the conventional wisdom was that decoupling capacitors should be placed as close as possible to the major active components. Within the past decade, the conventional wisdom for digital electronics on multilayered PCBs with planes (which is the model for modern high-speed digital design) has been that it is not generally necessary to relate the effectiveness of the decoupling capacitors to their distance with respect to the IC's, i.e., the decoupling capacitors behave in a global manner [18]. More recent work indicates that there are specific situations where the proximity of the decoupling capacitor to the IC can have a strong affect of the effectiveness of the capacitor [19]. Hence, there is a growing acceptance that there are specific design situations where it is beneficial for the capacitor to be placed "close" to an IC power pin.

Fig. 4 shows a conceptual configuration of an IC and a decoupling capacitor attached to a power bus. The current loop formed by the IC drawing current from the power bus and capacitor has three distinct regions of magnetic flux that define the inductance of this loop. The regions labeled  $L_{above}$  represent the inductance of the connection between IC and plane and between capacitor and plane. (The two  $L_{above}$  regions are not necessarily identical, but they are treated as such in this discussion.) The region labeled  $L_{below}$  represents the inductance of the portion of the current loop that exists between the power and ground planes.  $L_{below}$  has a self inductance component and a mutual inductance component which represents mutual coupling (transformer-like) between the two vias. The mutual inductance acts in opposition to the self-inductance and reduces the overall value of  $L_{below}$ . The total loop inductance encountered by the current flow from IC to capacitor is the sum of these inductances,

$$L_{Total} = 2L_{above} + L_{below} \quad (1)$$

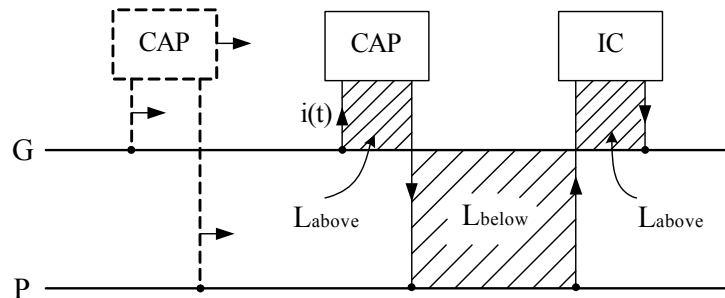


Fig. 4: Inductance "Above" and "Below" for connection to PDN.

If the capacitor were moved closer to the IC, as indicated by the dashed lines in Fig. 4, then the vias that form the boundaries of  $L_{below}$  become closer, the increased mutual magnetic coupling between these vias decreases  $L_{below}$  causing  $L_{total}$  to decrease. (The decrease in  $L_{below}$  due to mutual coupling is explained in the discussion of Fig. 5, later in this paper.) As stated earlier, the lower the inductance value, the faster the capacitor can supply and store charge and the more importance is attached to the distance of the decoupling capacitor from an IC in achieving effective decoupling capacitor behavior.

Therefore, this decrease in inductance should enhance the effectiveness of the decoupling capacitor and render decoupling effectiveness that is more apt to be location-dependant.

### Magnetic Coupling between Vias Can Affect Decoupling

The ability for rapid behavior is directly related to the inductance of the capacitor's interconnect and its ESL. However, two identical capacitors with identical interconnect may still differ in their abilities to exhibit local decoupling behavior. The reason for this is the degree of magnetic coupling that exists between the vias of the power/ground connections of the IC and the decoupling capacitor, as shown in Fig. 5. The mutual coupling between the vias reduces the overall interconnect inductance that determines the magnitude and rapidity of the charge supplied by the capacitor. (The reduction of overall inductance can be seen in Fig. 2, where the directions of the currents in the two vias produce magnetic flux in opposite directions in the region of mutual magnetic flux between the planes, thereby decreasing the total magnetic flux and the total inductance.) This mutual inductance can also increase the capacitor's effectiveness in reducing the PDN impedance and increase the maximum frequency for which this decoupling capacitor can be effective. A circuit representation of Fig. 2 is shown in Fig. 3.

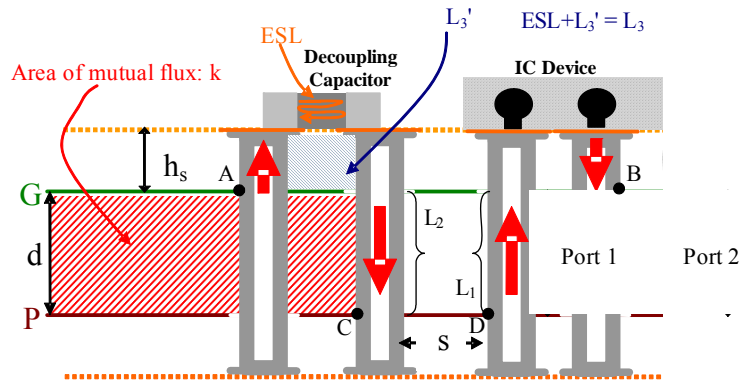


Fig. 5: Local Decoupling Inductance and Mutual Inductance.

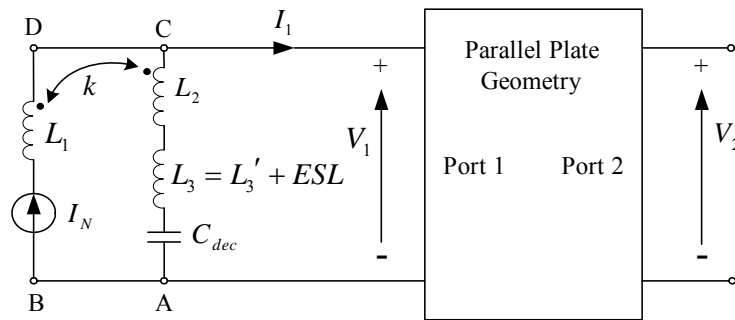


Fig. 6: Schematic Representation from Fig. 5.

The via pins connected to the same power layer (as seen in Fig. 5) are coupled through an area of mutual magnetic flux, resulting in a mutual inductance. The mutual inductance is seen in the equivalent circuit representation of the power delivery network in Fig. 6. This mutual inductance is a function of the IC/decoupling capacitor spacing ( $s$ ),

ground/power layer spacing, or thickness (d), and the proximity of both components to the edges of the board [16].

### Local Decoupling as Seen in the Frequency Domain

A majority of PCB PDN analysis has been done in the frequency domain. As an example, a PCB configuration that is a rectangle of dimensions 10 x 12 inches is analyzed. Port 1 simulates the location of a switching IC power pin. A movable decoupling capacitor is placed a distance,  $s$ , from Port 1. The capacitor has a value of 1  $\mu\text{F}$ , an ESL of 0.5 nH, and an ESR of 0.03  $\Omega$ . Port 2 represents a somewhat random location at which the voltage of the power bus may be observed. SPICE models for this PCB were extracted by means of a cavity model analysis tool with a circuit extraction feature [12, 13,]. This yields a lumped element model that includes the planes, ports and capacitors. The comparisons of the transfer impedance,  $|Z_{21}|$ , between Ports 1 and 2 for different capacitor distances from Port 1 are shown in Fig. 7 and Fig. 8, for frequencies above 1 GHz and for separation distances between power and ground planes of 10 and 35 mils, respectively. In this figure,  $L_3' = 0$ , which is an exaggeratedly low value, but which accentuates the effect of the mutual coupling. ( $L_3'$  is the interconnection inductance of the capacitor above the power bus planes, excluding the ESL of the capacitor, as indicated in Fig. 2.) The greater decreases in  $|Z_{21}|$  in the 35 mil structure, than in the 10 mil structure, implies that the 35 mil structure is a better structure for supporting capacitor location dependent local decoupling. Thicker power bus structures inherently provide more mutual coupling between vias, hence better support for local decoupling effects.

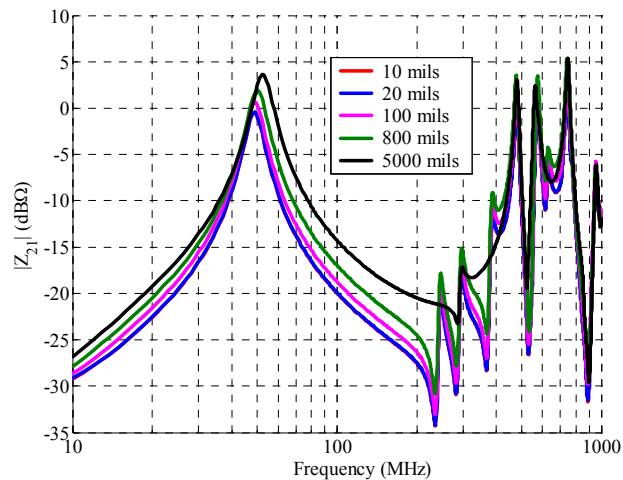


Fig. 7: Transfer Impedance for Dielectric Thickness = 10 mils.

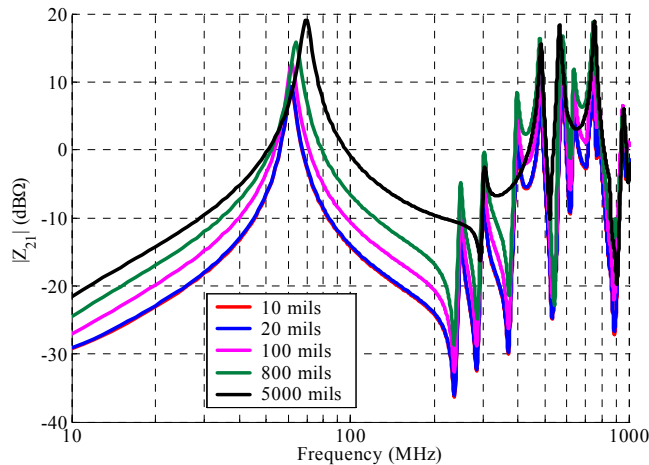


Fig. 8: Transfer Impedance for Dielectric Thickness = 35 mils.

Two factors play an important role in expression (2), i.e., the ratio  $L_3/L_2$  and the coupling factor  $k$ . The decrease in  $|Z_{21}|$  is negligible if the vias are so loosely coupled that there is no mutual coupling, or if  $L_3$  is much greater than  $L_2$ , i.e., the interconnect inductance of the via within the power/ground pair is much smaller than the sum of the interconnect inductance above the power/ground plane and the ESL. A relatively large ratio of  $L_3/L_2$  is easily achieved when the distance between the power and the ground plane is small; therefore thin power/ground PDN's often receive few benefits from a local decoupling strategy.

### Local Decoupling as Seen in the Time Domain

A different and possibly more intuitive way to examine PCB decoupling is to examine the phenomenon in the time domain. As discussed earlier, as an IC power pin switches very quickly from a high impedance state to a low impedance state (drawing current), the initial current must come from the portion of the power bus that is able to deliver charge in a nearly instantaneous manner. This part of the power bus is either a local decoupling capacitor or the stored charge between the power/ground-reference plane pair, or some combination of the two. If sufficient current is not available quickly enough from the decoupling capacitor (due to the inductance associated with the current path) then the voltage will dip substantially, causing a noticeably higher ripple voltage and EMI 'noise'. As the decoupling capacitor is moved farther away from the IC, the inductance associated with any current from the capacitor increases, resulting in less current provided and a higher noise level.

As shown in the previous section, the magnitude of the impedance in the frequency domain varied slightly as the capacitor is moved further away. However, this is only examining half the overall data and ignores the phase information. The time domain combines magnitude *and* phase, allowing a more complete picture of the real-world effects. To examine decoupling from the perspective of the time domain, the PCB configuration from earlier is re-examined. The simulated IC power pin, represented by Port 1, is represented by a time-dependent current source. This may not be the highest fidelity simulation of the switching power pin, but it is sufficiently accurate to be

illustrative. In this case, the current source with an isosceles triangular shape that has 2 ns duration with the peak reached at 1 ns.

Fig. 9 shows the resulting voltage at Port 2 versus time for various decoupling capacitor locations. The voltage waveforms shown are for the case of a power bus thickness of 35 mils and  $L_3' = 0$  (no interconnect inductance), an ESL value of 0.5 nH, and an ESR of 0.03 Ohms. The lack of interconnect inductance is unrealistic and exaggerates the effect of capacitor location but is used in this figure for illustrative purposes. The voltage peak at Port 2 during the first cycle of disturbance is much greater when the local decoupling capacitor is very far from Port 1 than it is when the capacitor is close to Port 1. This demonstrates that the location of the capacitor is important in determining the voltage swing, ripple voltage, at Port 2 as a result of state changes at Port 1. The initial cycle of the voltage disturbance is the time period during which the IC is in most need of rapidly delivered charge. The smaller voltage swing during the initial disturbance when the decoupling capacitor is located close to the IC ( $s$  is small) is indication that the IC's initial thirst for charge is more easily satisfied when the capacitor is close to the IC pin than when it is far away. This is consistent with the previous discussion. The values of the coupling coefficient,  $k$ , are noted for each value of distance between the vias.

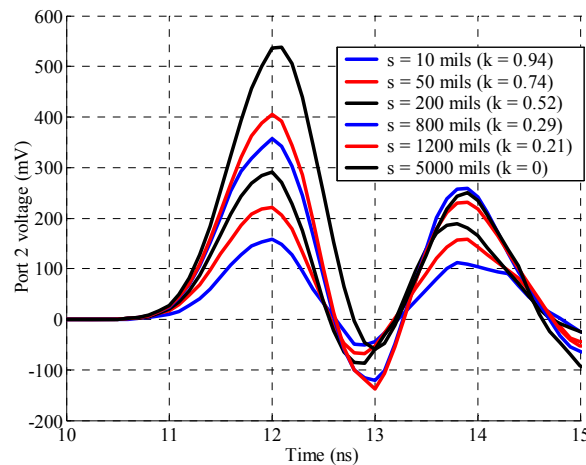


Fig. 9: Time Domain Noise Pulse for Different Decoupling Capacitor Distances.

The thirst for charge during the initial cycle of disturbance is important to the functionality of the IC. This time dependency of the voltage disturbance that comprises the power bus ripple is not so intuitively apparent when examining decoupling in the frequency domain [20]. It should also be noted that although the power bus planes and decoupling capacitor values and locations may be designed to supply charge to the IC and lower the power bus impedance, it can also be simultaneously true that insufficient charge is available to meet the demand of a particularly charge-thirsty IC. In this case, functional difficulties may result as the device may experience output waveform distortion. This is a topic beyond the scope of this paper.

Fig. 10 shows the change in peak voltage,  $\Delta V_p$ , in this initial disturbance period at Port 2 vs. distance between the capacitor and Port 1 (simulated IC power pin). The

capacitor has an ESL of 0.5 nH and an ESR of 0.03 Ohms. A larger change in peak voltage indicates a larger dependency on location of the capacitor. From Fig. 11, it is clear that for the thicker power bus,  $d = 35$  mils, the power bus voltage at Port 2 has a greater dependency on the proximity of the decoupling capacitor than the thinner power bus.

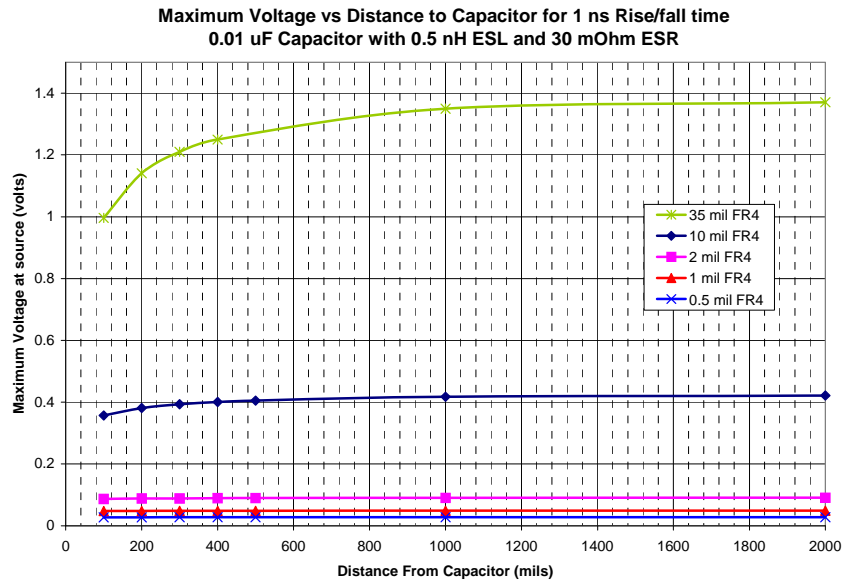


Fig. 10: Comparison of Maximum Time Domain Voltage for Different Decoupling Capacitor Distances and Dielectric Thicknesses.

Table 1 shows interesting effects when the power bus is not centered in the PCB stack-up as shown in Fig. 11. When positioning a power bus off-center in the stack-up, two power buses must be used in order to maintain PCB symmetry, or at least an identical two plane structure. The figure shows such a PCB with two power buses, each with a thickness of 10 mils. The IC is mounted on the obverse surface of the PCB with decoupling capacitors mounted on either observe or reverse sides of the board. The table shows the effects of moving a 10 mil power bus near the obverse surface of the PCB in terms of the  $L_3/L_2$  ratio. The decoupling capacitor on the obverse surface of the PCB has relatively short via lengths that form  $L_3'$ . The capacitor on the reverse side requires relatively long via lengths to reach the power bus connected to the IC. Table 1 shows that the ratios of  $L_3/L_2$  are vastly different depending on the surface upon which the capacitor is mounted. A capacitor ESL value of 0.5 nH was used when calculating  $L_3$ . When the capacitor is mounted on the obverse surface  $L_3/L_2$  is less than three, indicating the potential for effective local decoupling. However, when the capacitor is mounted on the reverse surface,  $L_3/L_2$  is greater than nine, indicating slim possibility of effective local decoupling. Hence, the position of the power bus in the PCB stack-up, along with placement of the capacitor can be very important in achieving effective local decoupling.

Fig. 12 shows the proper ways to place SMT decoupling capacitors near IC power pins in order to increase the mutual inductance between capacitor and IC vias, hence to take best advantage of local decoupling behavior. The four examples include all combinations of capacitors on top or bottom and power plane above or below the ground plane. (The

terminology “top” and “bottom” refer to the obverse and reverse sides of the PCB, which is often characterized by layer numbers in the PCB stack-up, layer 1 is near the top, etc.). The conclusion is that the IC power or ground pin and SMT capacitor should be placed so that the longer vias are proximate (regardless of there label as “power” or “ground”). This increases the mutual coupling and gives greatest weight to local decoupling behavior [21].

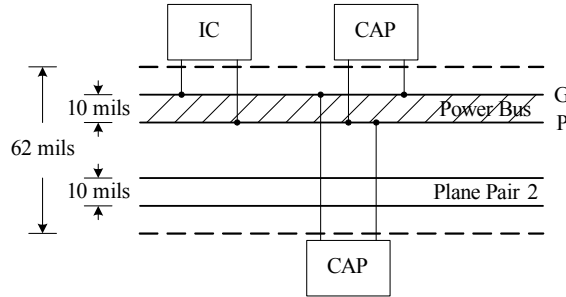


Fig. 11: Capacitor Mounting on Top/Bottom of PCB.

Table 1: Inductance from Capacitor Mounting on Top/Bottom of PCB.

DeCap Placement	L3' (nH)	L3/L2
Obverse	0.45	2.96875
Reverse	2.56	9.5625

Fig. 13 shows the “wrong” ways that one could place the decoupling capacitor, corresponding to Fig. 12(a). From this one can extrapolate the configurations shown in Fig. 13 to obtain the “wrong” ways to place the decoupling capacitor in those configurations. The rule is that if the longer vias are not proximate, the placement is wrong in the sense that the mutual inductance between the vias is not maximized; hence the potential for local decoupling is not maximized [16].

So, how close must a decoupling capacitor be to the IC pin to achieve effective local decoupling? No simple answer can be given to this question because the performance of a local decoupling capacitor depends on the power bus thickness,  $d$ , the inductance ratio,  $L_3/L_2$ , and the IC/capacitor spacing,  $s$ . As a rule of thumb, however, for a 35 mil thick power bus structure with a favorable  $L_3/L_2$  ratio (3, or less), a 3 dB decrease in both port voltage and power bus transfer impedance requires a capacitor to be within approximately 200 mils, or less of the IC power/ground pin.

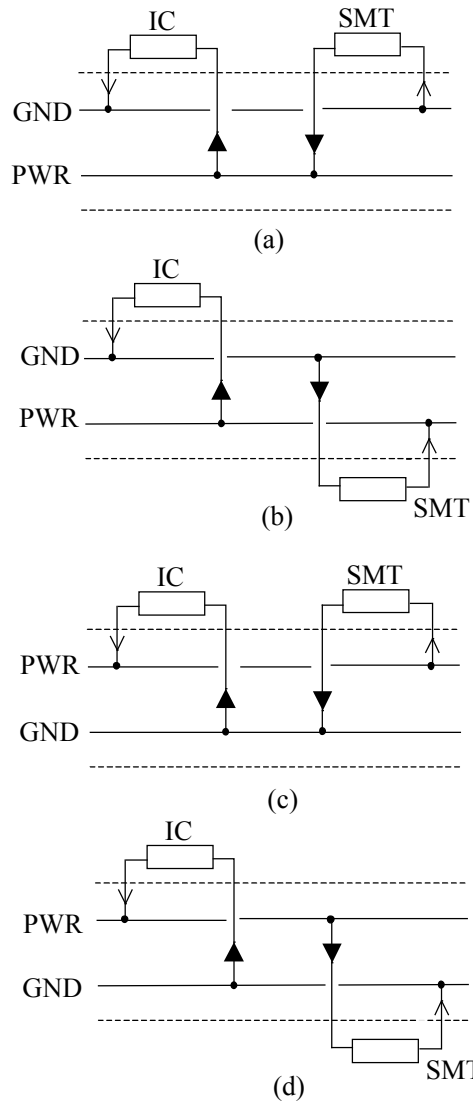


Fig. 12: Proper Capacitor Mounting Configurations.

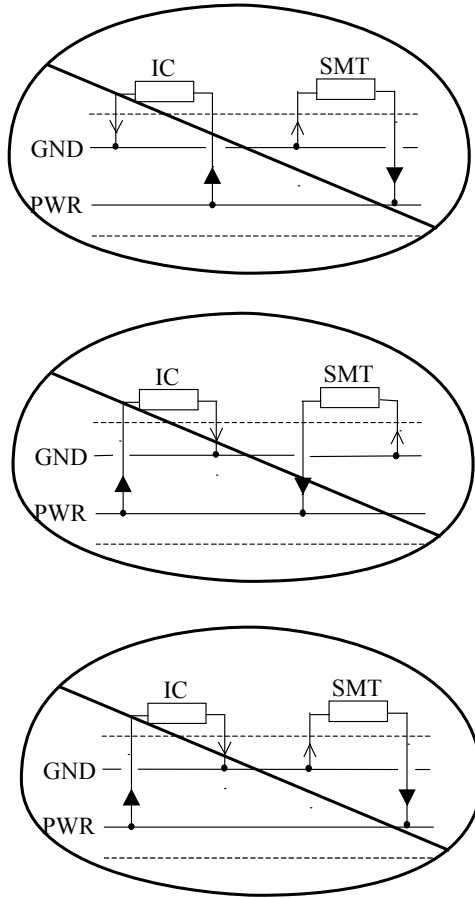


Fig. 13: Incorrect Capacitor Mounting Configurations.

### 3. Charge Depletion as Seen in the Time Domain

The charging hierarchy described in the first paragraph ranks the effectiveness of the storage elements constituting a power delivery network in terms of speed of charge delivery and amount of charge available for delivery. While the magnitude plots of measured or simulated S or Z-parameter data provide good insights regarding the frequency range of effectiveness for each of these charging elements, as shown in Fig.1, these plots always provide only half of the information, the other half being contained in the phase plots. More over, the charging-discharging cycles among the storage elements, hence the time constants associated with them, can be truly appreciated the time domain. Therefore, SPICE-based time-domain simulations are used in this section to provide the same insights shown in Fig.1 from a time domain prospective.

A concise sketch of the charging hierarchy described in the first paragraph is given in Fig14. Although, the PWR/GND plane model is represented only with the plane capacitance and inductance and all the storage elements seem to be connected to the same node, the circuit models employed in the time domain simulations take into account the distributed behavior and the relative locations of each charging element with respect to the others, as shown in Fig.15. Without loss of generality, the bulk capacitor is neglected

and the IC driver is replaced by a triangular current source sinking charge from the plane with a rise time of approximately 500 ps and a repetition of approximately 3 ns.

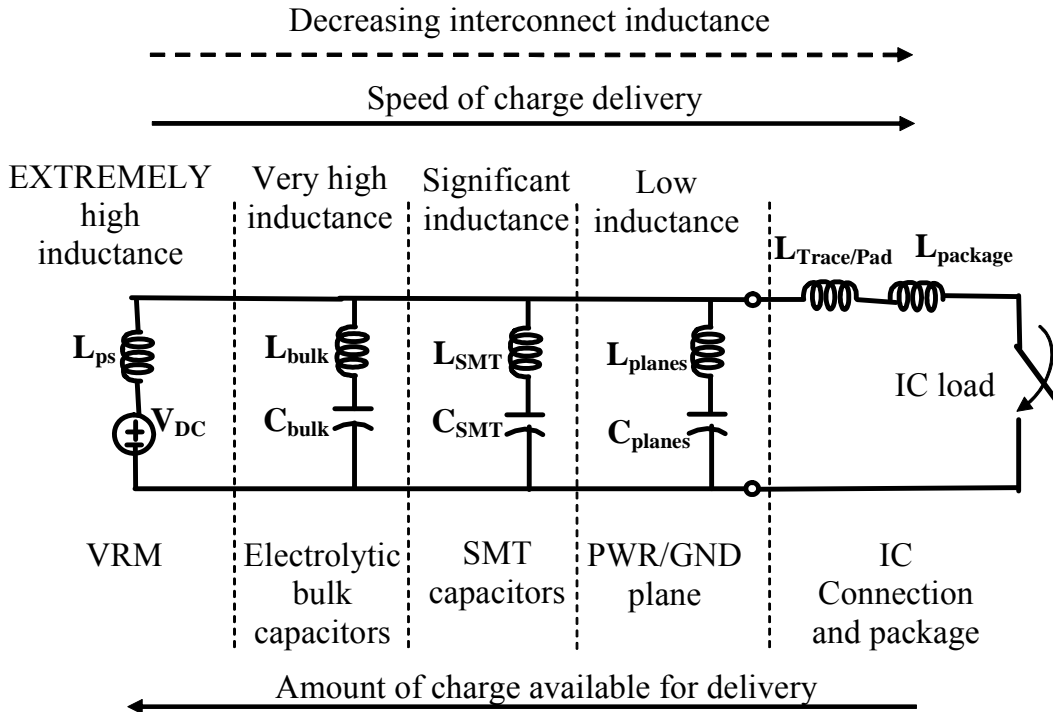


Fig.14: Charging hierarchy of a power delivery network.

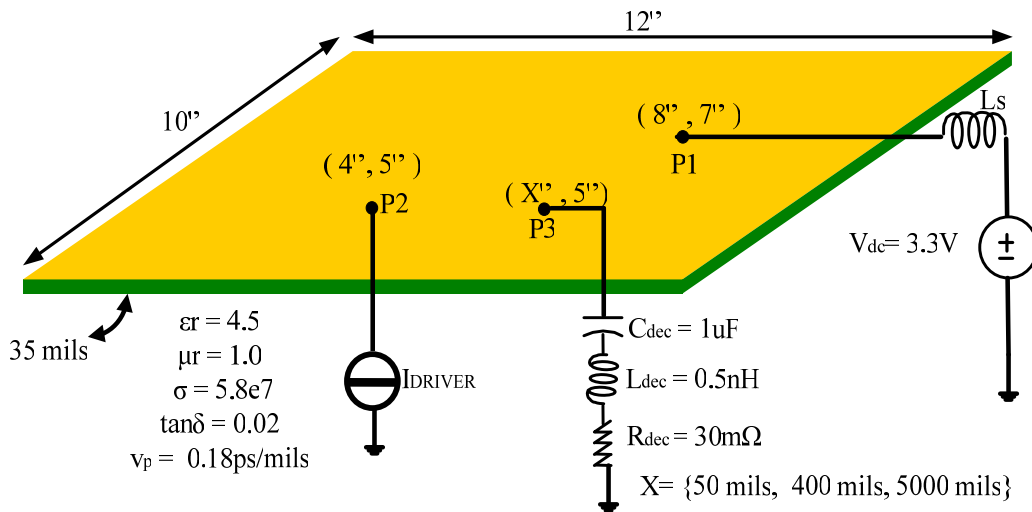


Fig.15: Board model under investigation.

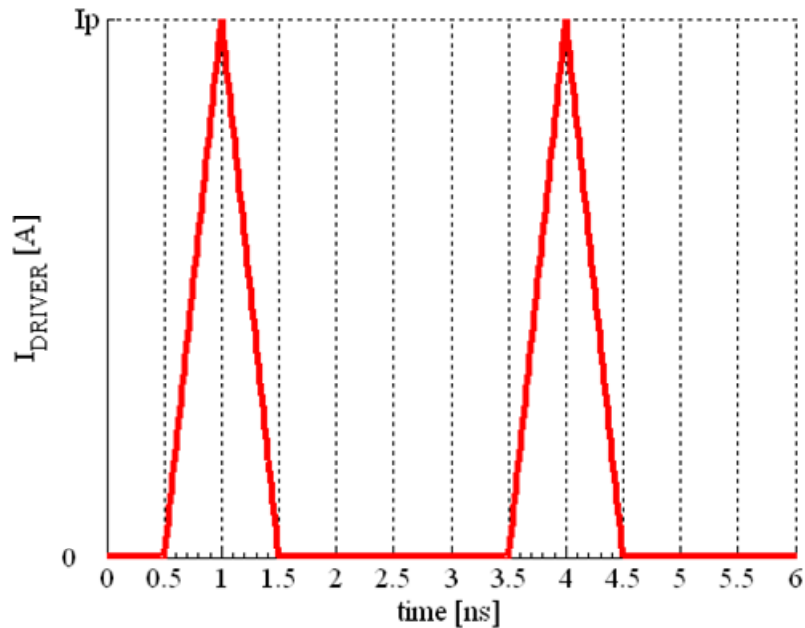


Fig.16: Current waveform sunk at Port 2. The peak current is chosen accordingly to the required time domain simulation settings.

#### The Inductance of the Port

The first set of time domain simulations deals with a phenomenon always observed in the frequency domain at high frequencies, and appreciated in the time domain during the early instants of time, i.e., the inductive behavior of a port connected between a pair of parallel planes. First of all, this frequency-domain time-domain duality is explained in terms of Fourier theory. The frequency domain voltage observed at Port 2 of

Fig.15 is equal to the Fourier Transform of the current waveform exciting Port 2 multiplied by the impedance seen looking into the pair of plane at the same port. This self-impedance is shown in Fig. 17 and it is characterized by a distinctive 20 dB/dec slope. This behavior corresponds to an inductive element and not to a capacitive element and a distinctive  $L \, di/dt$  behavior is observed in Fig.18(a) and (b), when simulating the circuit for the board model of Fig.15 in the time domain. In this set of simulations, the peak current  $I_p$  is chosen to be approximately 120 mA, the base of the triangles are 1ns and 2ns, and the repetition are 3ns and 4ns, respectively. These values are chosen to ensure a charge demand from the current source at every cycle of approximately 5‰ and 1‰ of the overall charge available, respectively. Hence, the pair of planes are not stressed the inductive behavior becomes the most relevant feature to be observed. The amount of charge available from the plane is about 12nC ( $3.3V \times 3.5nF$ ), whereas the amount of charge depleted from the planes each cycle is about 60pC and 120pC, respectively. Finally, the decoupling capacitor is disconnected during this first set of simulations.

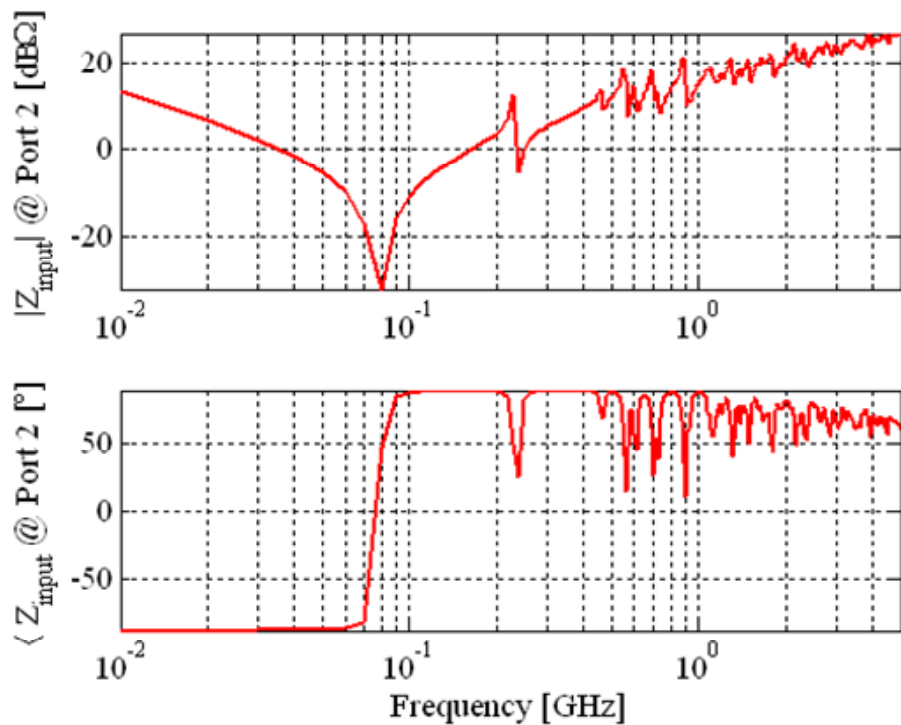


Fig.17: Self-impedance, magnitude and phase, looking into Port 2 of Fig.15.

As soon as the voltage across the planes is settled to about 3.3 V, the current (noise) source is switched on with the shape and the repetition shown in Fig.18(a) and (b) - lower red curves. The amount of charges depleted from the plane is very small, hence the mean value of the voltage does not deviate significantly from the steady state value of about 3.3V. On the other hand, the amount of charge per unit time, i.e., the current flowing into Port 2 is able to create an  $Ldi/dt$  type of voltage drop. When the current is on the rising edge, the voltage decreases, when the current is on the falling edge, the voltage swings back overshooting above the mean value of 3.3V. The inductive behavior of the port is further demonstrated by observing halved voltage dips and peaks, when the triangle base is doubled from 1 ns to 2 ns, Fig. 18(b) vs. Fig.18(a).

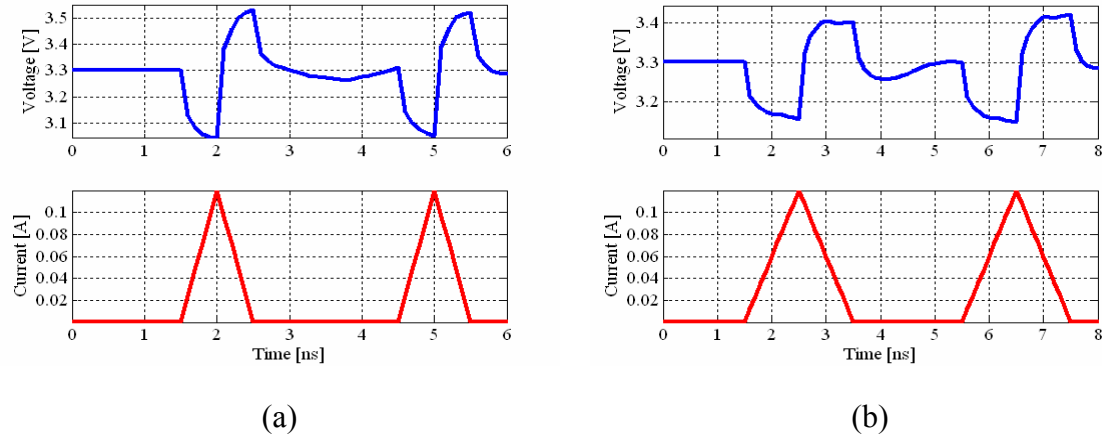


Fig.18: Triangular current at Port 2 for (a) 1 ns base; (b) 2 ns base. The corresponding inductive voltage drop is observed at the terminals of Port 2.

### The Effect of the Inductance $L_s$

The second set of time domain simulations deals with the charge/discharge issues associated with only the voltage supply and current source, connected at Port 1 and Port 2, respectively. The charge depletion from the plane needs to be large, now, in order to appreciate the charge/recharge mechanism. The peak current is then increased to 5A and each triangle of 1 ns encloses approximately 22% of the overall charge available between the pair of planes. When the current driver is switched on, the voltage across the plane starts decreasing from 3.3 V. Every cycle the voltage decrease due to a constant drawing of charge at Port 2. The voltage sag stops when the voltage supply senses this reduction and it starts supplying charges to restore the 3.3V steady state voltage. An oscillation is then triggered due to the series inductance of the voltage supply and the capacitance of the planes. This oscillation is slowly damped until a new steady state is reached again. The voltage across the planes for three configurations characterized by three different values of voltage supply series inductance are shown in Fig.19. The oscillation frequencies for each of the cases given in Fig.19 are calculated and reported in Table 2.

Table 2: Resonant frequencies associated to oscillations observed in Fig.19.

$L_s$ ( $C_p = 3.5\text{nF}$ )	$f_{res} = \frac{1}{2\pi\sqrt{L_s C_p}}$	$\tau = \frac{1}{f_{res}}$
1nH	~ 83MHz	~ 12ns
10nH	~27MHz	~37ns
50nH	~12MHz	~83ns

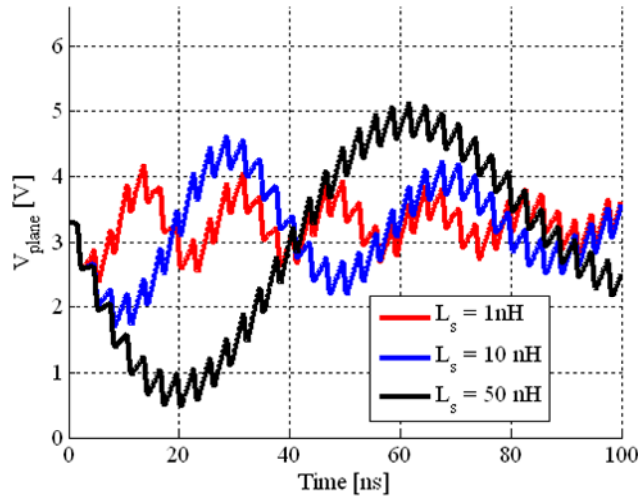


Fig.19: Voltage observed across the plane pair of the board model given in Fig.15 for different voltage supply series inductance.

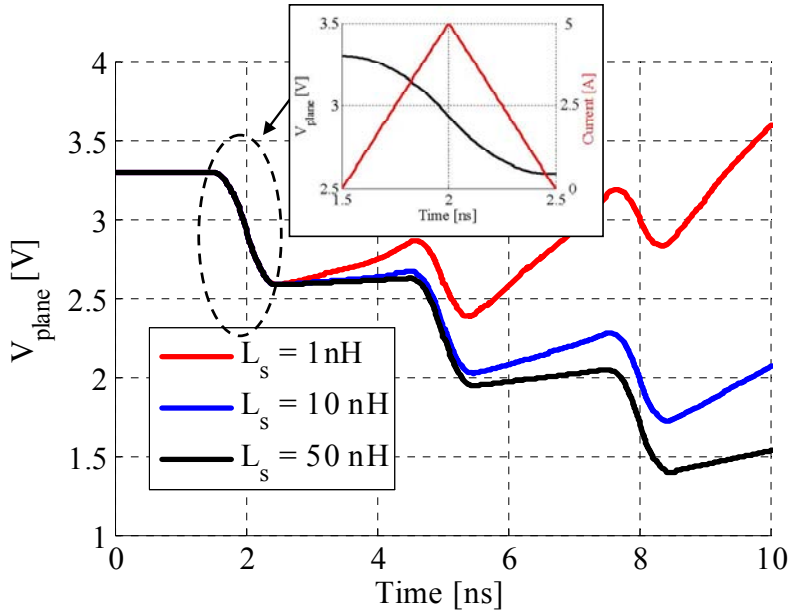


Fig.20: Close up of the voltage given in Fig.19.

The close up view shown in Fig.20 provides additional insights on the charge depletion mechanism due to the current sunk from the driver. When the current driver is switched on at  $t$  equal to 1.5 ns, the voltage between the planes (at this location) starts decreasing in a quadratic fashion. During the duration of the first current pulse - 1ns - the voltage must sag of about 22%, since the charge associated with each triangle is about 22% of the total plane charge and there are no other source of charges in a radius of 1 ns in proximity of the driver. The level reached by the voltage across the plane at  $t$  equal to 2.5 ns is in fact 2.58V, which is approximately 22% smaller than the steady state value of 3.3V.

As soon as the disturbance reaches the voltage supply, this storage elements reacts by supplying charges in order to re-establish an equilibrium. Depending upon the value of series source inductance, this charge supply is slowed down and the voltage across the plane continues to sag especially for the configurations characterized by large values of series inductance. On the other hand, when the voltage supply has a low value of series inductance, this storage element can supply charge as fast as the velocity of propagation allows it.

### The Benefits of Decoupling

The conclusions drawn from the previous sections are very helpful to introduce the final set of time domain simulations. These are carried out by employing a current driver with a triangular pulse of 5A peak current and a base of 1 ns with 3 ns repetition, a 3.3V voltage supply with a 50nH series inductance and a decoupling capacitor of 1 uF with 30mΩ ESR and 0.5nH ESL at 50 mils, 400 mils and 5000 mils from the current source along the x direction as shown in Fig. 15. The system is charged up until all the components connected to the planes have reached a steady state voltage of about 3.3V, then the time varying current (noise) source is started.

A first comparison between the case with no decoupling capacitor and decoupling capacitors at different locations is shown in Fig.21. As expected, placing a decoupling capacitor across the pair of planes helps maintaining the voltage swing within tighter bounds. Several charge/discharge mechanisms are now possible, i.e., from the voltage supply to the planes, from the voltage supply to the decoupling capacitor from the decoupling capacitors to the planes. More over, each of these mechanisms has its own characteristic time constant. For instance, the voltage supply – plane pair charge exchange mechanism is characterized by the same time constant described before for a 50nH source inductance, i.e., approximately 83 ns. The voltage supply – decoupling capacitor charge exchange mechanism is characterized by a time constant of about 1400ns ( $f_{res} = 0.7\text{MHz}$  from  $C = 1\mu\text{F}$  and  $L = 50\text{nH}$ ). Finally the decoupling capacitor – plane pair charge exchange mechanism is going to be characterized by a time constant in the order of 13ns, due to the inductance of the full capacitance interconnection, approximately 1.2nH, and the plane capacitance, approximately 3.5nF. The capacitance ratio between the decoupling capacitor and the pair of planes is about 300, hence the charged decoupling capacitor is like a constant voltage source with a small interconnect inductance for the parallel plane.

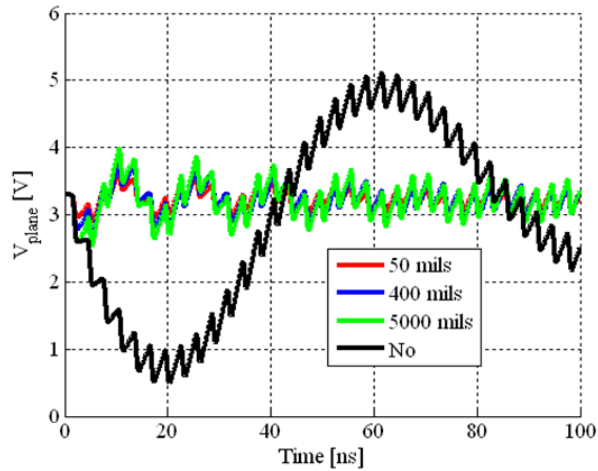


Fig.21: Voltage observed across the plane pair of the board model given in Fig.15 for different locations of the decoupling capacitor or no decoupling capacitor.

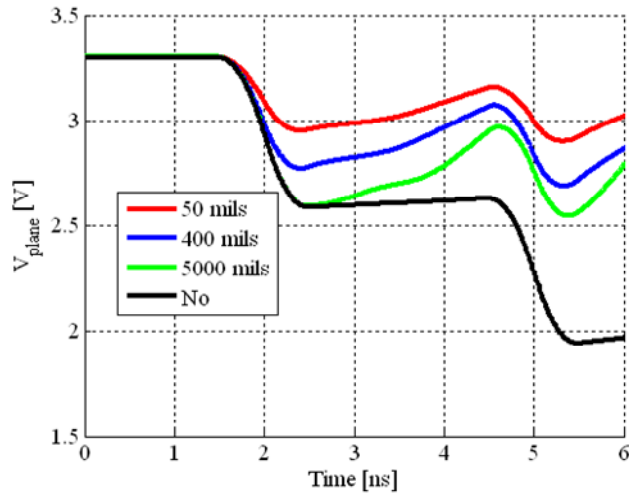


Fig.22: Close up of the voltage given in Fig.21.

The expanded view of the early time (first few current pulses) shown in Fig. 22 provides additional insights regarding the effectiveness of the decoupling capacitor location to replenish the charge locally across the pair of planes. For instance, when the decoupling capacitor is located within 50 mils it is able to begin to replenish the charge within the first few hundreds of picoseconds, and the nominal voltage only decreases to about 2.95 volts. As another example, when the decoupling capacitor is located five inches away, it can begin to replenish the local charge only after a much longer time, and the voltage decreases to approximately 2.6 volts and only raises to about 2.95 volts before the next current pulse occurs. If the second current pulse had occurred sooner, then the voltage would have not risen as high. In the case of no decoupling capacitor, the charge must be replenished from the supply (which is highly inductive), and the charge never reaches this point in the planes before the second current pulse occurs, further depleting the local charge.

## 4. Summary

This paper has provided a discussion of the various aspects of the decoupling capacitor and how it relates to providing charge to ICs on PCBs. Signal integrity engineers and EMC engineers often view the role of a decoupling capacitor from different points of view, but the capacitor actually functions to serve both purposes.

The importance of the value of the decoupling capacitor and more importantly, the amount of inductance introduced by physically connecting the capacitor to the PCB planes is examined. This connection inductance dominates the performance of the capacitor, making the actual value of capacitance of small importance for most real-world PCBs.

The role of the capacitor as a charge storage device, and the amount of time needed to provide that charge is examined to indicate if the location of the decoupling capacitor is important. Again, the connection inductance dominates the capacitor's ability to provide the charge to an IC *during the time it is needed*, making the location of the decoupling capacitor seem unimportant, since the inductance associated with the capacitor's charge will usually be significantly higher than the charge stored between the planes.

And finally, the role of the capacitor as a charge source to recharge the depleted planes is discussed, and the location of the decoupling capacitor is shown to be very important to maintaining a small noise voltage fluctuation in the local area near the IC drawing the current.

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